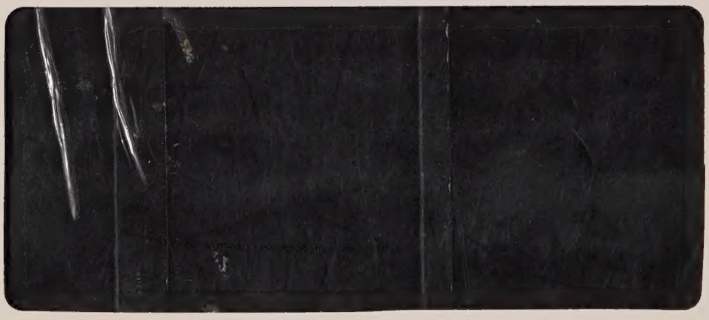
03M05B5

technical manual

ELDORADO

ELDORADO ELECTRODATA CORPORATION

601 CHALOMAR ROAD • CONCORD, CALIF. 94520 U.S.A. • TEL. (415) 686-4200 • TWX 910-481-9476



TECHNICAL MANUAL

MODEL 970

MICROWAVE FREQUENCY COUNTER

ELDORADO ELECTRODATA CORP.
601 Chalomar Road
Concord, California 94520
Telephone: 415-686-4200
TWX: 910-481-9476

Digitized by the Internet Archive
in 2025

https://archive.org/details/manualsplus_07418

INITIAL TESTING OF UNHEATED CRYSTAL OSCILLATORS (Non-Ovenized)

Extensive testing of the aging rates of the unheated type crystal oscillators has recently been completed. Based on this research, verification of the published aging rate can be accurately determined within a reduced time interval. The following procedure will validate the initial aging specifications.

1. Attach a thermometer or temperature sensing device to the crystal case.

2. Apply instrument power for a twenty four hour period.

3. Measure the crystal's external temperature to within 1° C.

4. Measure the crystal oscillator's frequency to within 1 part in 10^7 (0.1 Hz).

5. After one week's continuous operation again measure the crystal temperature and output frequency.

6. The two frequencies will be within 2 parts in 10^6 (2 Hz), taking into consideration a temperature coefficient of $\pm 0.5 \times 10^{-6}$/° C.

7. The above test confirms the published oscillator specifications.

Return Material Authorization (RMA)

Complete the RMA card and enclose with the returned instrument. To obtain RMA number call or write to:

ELDORADO ELECTRODATA
601 Chalomar Road
Concord, California 94520
c/o Customer Service
Tel: (415) 686-4200
TWX: 910-481-9476

RETURN MATERIAL AUTHORIZATION			RMA NO
NAME			DATE
COMPANY			PHONE
SHIPPING ADDRESS			MODEL
CITY	STATE	ZIP	SERIAL NUMBER
REASON FOR RETURN			
PURCHASING AGENT			
BILLING ADDRESS			
Eldorado Electrodata Corp., 601 Chalomar Road, Concord, California 94520			

In Eldorado's efforts to produce the best in support literature, we would like to know how useful you, our customer, find the Technical Manual. Please complete this questionnaire and drop it in the mail box.

Thank you,
Publications Department

1. Instrument Model_____. Serial Number_____.
2. Do you operate ☐ or maintain this instrument ☐ ?
3. After reading the Specifications and Introduction Section did you feel that you had an adequate idea of the instrument's capabilities? ..... Yes ☐ No ☐
4. After reading the Operating Instructions were you able to operate the instrument to your satisfaction? ..... Yes ☐ No ☐
5. Were you able to calibrate the instrument with the calibration procedure? ..... Yes ☐ No ☐
6. Are you able to find the information you need on replacement parts in the parts list? ..... Yes ☐ No ☐
7. What would you like to see in future Eldorado Technical Manuals?

Comments please_____

Product Line Inquiry Card

Use this convenient postage paid card for instrumentation information request.

Name_____ Date_____

Title_____ MS_____

Company_____ Tel: ( ) _____

Address_____ City_____

State_____ Zip_____

Please:

Contact me regarding_____

Do not contact me, but send literature on_____

- ☐ Time Interval Counters
- ☐ Time Code Instrumentation
- ☐ Computer and Data Terminals
- ☐ Frequency Counters
- ☐ Microwave Frequency Counters
- ☐ Continuous Reversing Ratiometers
- ☐ Digital Delay Generators
- ☐ Digital Volt/Ohm Meters
- ☐ Power Pack
- ☐ Universal Counter/Timers

My application requirements are_____

FIRST CLASS
PERMIT NO. 205
CONCORD
CALIFORNIA

BUSINESS REPLY MAIL

No postage stamp necessary if mailed in the United States

POSTAGE WILL BE PAID BY

Eldorado Electrodata Corp.
601 Chalomar Road
Concord, California 94520

FIRST CLASS
PERMIT NO. 205
CONCORD
CALIFORNIA

BUSINESS REPLY MAIL

No postage stamp necessary if mailed in the United States

POSTAGE WILL BE PAID BY

Eldorado Electrodata Corp.
601 Chalomar Road
Concord, California 94520

warranty

Eldorado instruments are warranted during a period of one year from date of shipment to original purchaser to be free from defects in material and workmanship. The liability of Eldorado under this warranty is limited to replacing or repairing any instrument or component thereof which is returned by Buyer and has not been subjected to misuse, neglect, improper installation, repair, alteration, or accident. Eldorado shall have the right of final determination as to the existence and cause of a defect. In no event shall Eldorado be liable for collateral or consequential damages. In order to expedite the rapid turnaround of your unit, please obtain a Returned Material Authorization (RMA) number by contacting the Customer Service Department. In all correspondence or telephone calls, a model number and serial number is required. Address all correspondence to Customer Service Department, Eldorado Electrodata Corporation, 601 Chalomar Road, Concord, California 94520, Phone (415) 686-4200, TWX 910-481-9476.

The instrument should be shipped prepaid with the return form attached to the packing container. When the instrument is repaired it will be returned to you best way prepaid.

This warranty is in lieu of any other warranty, express, implied, or statutory, and no agreement extending or modifying it will be binding upon Eldorado unless in writing and signed by a duly authorized officer.

RECEIVING INSPECTION

Every Eldorado instrument is carefully inspected and is in perfect working order at the time of shipment. Each instrument should be checked as soon as received. If the instrument is damaged in any way or fails to operate, a claim should immediately be filed with the transportation company. In any case where damage occurs in transit with the instrument in packing case, Eldorado's obligations under warranty are dependent on the customer's immediately notifying the carrier so that inspection can be made and a claim filed.

REPAIR SERVICE

Experienced service personnel and special test equipment are available at the factory to perform any necessary repairs. Every effort will be made to expedite the repair of instruments returned for servicing. Repair work will be performed only upon receipt of a written purchase order or authorization. Utilize the same procedure for returning an instrument for service as for warranty return. After receipt of the unit the Customer Service Department will issue a quotation of repair costs for your approval.

1/70

TABLE OF CONTENTS

		PAGE
SECTION 1	GENERAL INFORMATION	
1.1	Introduction	1-1
1.2	Sampling Technique	1-1
1.3	Specifications	1-2
SECTION 2	INSTALLATION AND OPERATION	
2.1	Introduction	2-1
2.2	Unpacking and Inspection	2-1
2.3	Power Requirements	2-1
2.4	Incoming Confidence Check	2-2
2.5	Installation	2-3
2.6	Front Panel Description	2-5
2.7	Rear Panel Description	3-7
2.8	Operation	2-9
SECTION 3	THEORY OF OPERATION	
3.1	Introduction	3-1
3.2	Sampling Principle	3-1
3.3	Sampling Technique	3-1
3.4	Block Diagram Analysis	3-7
3.5	Detailed Theory of Operation	3-22
3.6	Specialized Components	3-39
SECTION 4	MAINTENANCE - CALIBRATION	
4.1	Introduction	4-1
4.2	Periodic Maintenance	4-1
4.3	Calibration	4-2
4.4	Internal Adjustments	4-5
4.5	Repair	4-12
4.6	Repair Techniques	4-12
4.7	Integrated Circuit Equivalents	4-14
SECTION 5	SCHEMATICS AND RELATED DRAWINGS	

LIST OF ILLUSTRATIONS

FIGURE	TITLE	PAGE
1-1	Sampling Technique	1-2
2-1	Front Panel	2-5
2-2	Rear Panel	2-7
3-1	Input Block Diagram	3-2
3-2	Countdown Output	3-2
3-3	Sampler Output Without Slewing	3-3
3-4	Sampler Output With Slewing	3-3
3-5	Vector Addition of f/N and Δf	3-4
3-6	Addition of f/N and Δf	3-6
3-7	Countdown Circuit Block Diagram	3-8
3-8	Frequency Synthesizer Block Diagram	3-10
3-9	Sampler Block Diagram	3-11
3-10	Parity Block Diagram	3-15
3-11	Time Base Block Diagram	3-17
3-12	120 MHz DCU Block Diagram	3-19
3-13	Simplified Block Diagram	3-21
3-14	Tunnel Diode	3-39
3-15	Step Recovery Diode	3-40
4-1	Oscillator Test Configuration	4-3
4-2	Oscillator Component Location	4-4
4-3	Power Supply Adjustment Location	4-6
4-4	+4 Volt Voltage Divider	4-6
4-5	Countdown Adjustment Location	4-8
4-6	Frequency Synthesizer Adjustment Location	4-10
4-7	Synthesizer Waveforms	4-10
4-8	Sampler Bias Adjustment Location	4-11
4-9	MC717P Equivalent	4-14
4-10	MC724P Equivalent	4-15
4-11	MC725P Equivalent	4-15
4-12	MC839P Equivalent	4-16
4-13	MC839P Equivalent	4-17

4-14	MC771P Equivalent	4-18
4-15	MC786P Equivalent	4-19
4-16	MC789P Equivalent	4-20
4-17	MC793P Equivalent	4-20
4-18	MC790P Equivalent	4-21
4-19	MC791P Equivalent	4-22
4-20	CμL 9958 Equivalent	4-23
4-21	CμL 9959 Equivalent	4-24
4-22	CμL 9960 Equivalent	4-25
4-23	MC1004P (L) Equivalent	4-26
4-24	MC1013P (L) Equivalent	4-27
4-25	MC1018P (L) Equivalent	4-28
4-26	MC1023P (L) Equivalent	4-29
4-27	MC1027P (L) Equivalent	4-30
4-28	MC1437L Equivalent	4-31
4-29	CA3046 Equivalent	4-32
4-30	MC3062P (L) Equivalent	4-33
5-1	Internal Orientation	5-1
5-2	Logic Board Component Location	5-2
5-3	Mother Board Component Location	5-3
5-4	120 MHz DCU Component Location	5-4
5-5	Countdown Component Location	5-4
5-6	Frequency Synthesizer Component Location	5-5
5-7	Input Sampler Component Location	5-5
5-8	Coaxial Cable Terminations	5-6

Schematic, Input Amp Power Divider and Misc. Control Circuits	C-11-06052
Schematic, Countdown	C-11-06414
Schematic, Frequency Synthesizer	C-11-05821
Schematic, Sampler	C-11-05823
Schematic, AF Phase Shifter	B-11-06045
Schematic, Error Counter and Ramp Generator	C-11-06046
Schematic, Fine and Coarse Parity	C-11-06049
Schematic, Time Base	D-11-06044

List of Illustrations (Continued)

Schematic, Control and Reset	C-11-06048
Schematic, 120 MHz DCU	C-11-06051
Schematic, Count Chain	D-11-06053
Schematic, Power Supply	C-11-06047

LIST OF TABLES

TABLE	TITLE	PAGE
1-1	Specifications	1-2
2-1	230 Volt Operation	2-2
2-2	Self-Test	2-3
2-3	Option R5 Rack Mount Assembly	2-4
2-4	Front Panel Description	2-5
2-5	Rear Panel Description	2-8
2-6	Basic Operation	2-9
3-1	Power Levels	3-20
4-1	Recommended Test Equipment	4-1
4-2	Periodic Maintenance	4-2
4-3	Oscillator Calibration	4-3
4-4	Power Supply Calibration	4-5
4-5	Countdown Bias Adjustment	4-7
4-6	Frequency Synthesizer Balance Adjustment	4-9
4-7	Input Sampler Bias Adjustment	4-11

SECTION 1

GENERAL INFORMATION

SECTION 1

GENERAL INFORMATION

1.1 INTRODUCTION

The Eldorado Model 970 is a direct microwave frequency counter with an effective range from 20 Hz to 3.2 GHz. Measurement is completely automatic requiring only the appropriate selection of one of three operating frequency ranges. A unique sampling technique eliminates the errors inherent with the heterodyne or transfer oscillator method of high frequency measurement. The simplicity of operating controls combined with a nine digit display enable less-skilled operators the ability to make virtually error-free measurements void of the monotonous task of hand calculations.

1.2 SAMPLING TECHNIQUE

Due to the frequency limitations of solid-state flip-flop circuitry above 200 MHz, an alternate method for high frequency measurement is necessitated. The Eldorado Model 970 employs a sampling technique to realize frequency measurements to 3.2 GHz.

In simplest terms, the sampling technique utilizes a subharmonic of the applied input frequency. Referring to Figure 1-1, assume an unknown input frequency (f) and its resultant sub-multiple (f/N). The counter passes the subharmonic to the count gate and solves for the harmonic multiple N. Once N is determined, the time base is expanded by the factor N and directed to the count gate as the count enable signal. The count chain now counts the subharmonic f/N for a period equal to the normal time base times N. The mathematical result is (f/N) (N) or f, the value of the applied input frequency.

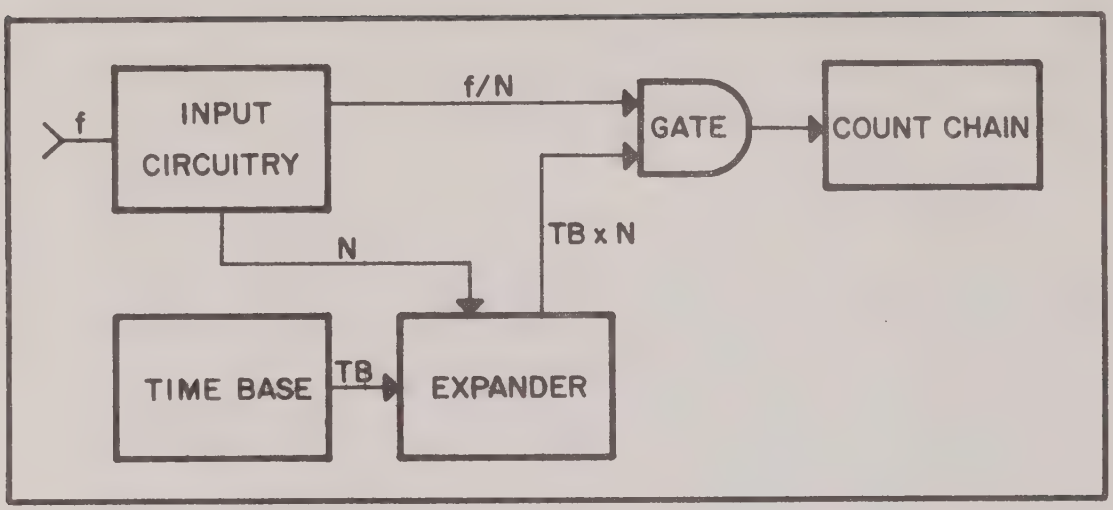


FIGURE 1-1

SAMPLING TECHNIQUE

1.3 SPECIFICATIONS

Table 1-1 lists the specifications for the Eldorado Model 970 Microwave Frequency Counter.

TABLE 1-1

SPECIFICATIONS

FREQUENCY MEASUREMENTS	
Range:	20 Hz to 3.2 GHz in three overlapping bands on a single input.
Low Band:	20 Hz to 120 MHz.
Mid Band:	110 MHz to 700 MHz.
High Band:	0.6 GHz to 3.2 GHz.
Accuracy:	± 1 count ± oscillator stability.
Self Test:	Counts internal 1 MHz oscillator on low band.

TABLE 1-1 (Continued)

Resolution:	Switch selectable; 0.1 Hz, 1.0 Hz, 10 Hz, 0.1 kHz and 1.0 kHz on low band; 10 Hz, 0.1 kHz and 1.0 kHz on mid and high bands.
Count Time:	
Low Band:	1 ms to 10 s by front panel RESOLUTION switch.
Mid and High Bands:	1 kHz resolution; less than 200 ms. 100 Hz resolution; less than 1.1 s. 10 Hz resolution; less than 10 s.
TOTALIZING MEASUREMENTS (COUNT)	
Rate:	120 MHz maximum counting rate.
Maximum Count Displayed:	999999999.
Count On:	Continuous until count off, cumulative until manual reset.
Count Off:	Input inhibited, accumulated count retained until manual reset.
Accuracy:	Absolute.
INPUT CHARACTERISTICS	
Sensitivity:	Low band; -13 dBm (50 mV rms). Mid band; -7 dBm (100 mV rms). High band; -7 dBm (100 mV rms) to 2.4 GHz, -1 dBm (200 mV rms) from 2.4 to 3.2 GHz.
Maximum Operating Input:	+10 dBm (700 mV rms).
Maximum Non-damaging Input:	+20 dBm (2.2V rms).

TABLE 1-1 (Continued)

Impedance:	50 ohms (nominal).
VSWR:	Less than 2.5:1 (typical).
Connector:	Front panel mounted type TNC connector.
TIME BASE	
Frequency:	1 MHz.
Stability:	1 part in 10^6 per month after 30 days continuous operation.
Temperature:	±0.002% from 0 to +50° C.
Oscillator Monitor:	BNC type UG1094 connector, rear panel mounted.
GENERAL	
Display Time:	Variable from approximately 0.1 seconds to 10 seconds or infinite.
Storage On:	Counter displays most recent measurement.
Storage Off:	Visual display of measurement in progress.
Reset:	Manual; front panel pushbutton switch. Remote; contact closure to ground on rear panel RESET connector. Automatic; reset occurs automatically at end of display period.
Display:	Nine numerical display indicators. Display reads in kHz with automatically positioned decimal point.

TABLE 1-1 (Continued)

Temperature	Operating; 0° C to +50° C. Storage; -55° C to +80° C.
Power Requirements:	115 or 230Vac (±10%) switch selectable. 50-60 Hz, 60 watts.
Dimensions:	3.5" x 16.8" x 15" (HxWxD).
Weight:	16 lbs net. 22 lbs shipping.
OPTIONS	
Option C:	Internal temperature controlled crystal oscillator (115Vac operation). Short term stability; 7 parts in 10^9 (average) for a 10 second period. Long term stability; 3 parts in 10^8 per week after 45 days continuous operation. Temperature; 5 parts in 10^9 per ° C over a temperature range of 0° C to +50° C.
Option C1:	Internal temperature controlled crystal oscillator (230 volt ac operation). Short term stability; 7 parts in 10^{-9} (average) over a 10 second period. Long term stability; 3 parts in 10^8 per week after 45 days continuous operation. Temperature; 5 parts in 10^{-9} per ° C over a temperature range of 0° C to +50° C.
Option D:	Internal temperature controlled crystal oscillator (115 volt ac operation). Short term stability; 5 parts in 10^{10} (peak to peak) over a 7 minute period. Long term stability; 2 parts in 10^9 per day after 48 hours continuous operation.

TABLE 1-1 (Continued)

Option D: (Continued)	Temperature; 2 parts in 10^{10} per ° C (average) over a temperature range from 0° C to +50° C. Retrace; 5 parts in 10^{9} of previous frequency after 60 minutes operation following a 24 hour off-time.
Option D1:	Internal temperature controlled crystal oscillator (230 volt ac operation). Short term stability; 5 parts in 10^{10} (peak-to-peak) over a 7 minute period. Long term stability; 2 parts in 10^{9} per day after 48 hours continuous operation. Temperature; 2 parts in 10^{10} per ° C (average) over a temperature range from 0° C to +50° C. Retrace; 5 parts in 10^{9} of previous frequency after 60 minutes operation following a 24 hour off-time.
Option E:	Internal temperature controlled crystal oscillator (115 volt ac operation). Short term stability; 5 parts in 10^{10} (peak-to-peak) over a 7 minute period. Long term stability: 1 part in 10^{9} per day after 48 hours continuous operation. Temperature; 2 parts in 10^{10} per ° C (average) over a temperature range from 0° C to +50° C. Retrace; 5 parts in 10^{9} of previous frequency after 60 minutes operation following a 24 hour off-time.
Option E1:	Internal temperature controlled crystal oscillator (230 volt ac operation). Short term stability; 5 parts in 10^{10} (peak-to-peak) over a 7 minute period. Long term stability: 1 part in 10^{9} per day after 48 hours continuous operation. Temperature; 2 parts in 10^{10} per ° C (average) over a temperature range from 0° C to +50° C. Retrace; 5 parts in 10^{9} of previous frequency after 60 minutes operation following a 24 hour off-time.

TABLE 1-1 (Continued)

Option N:	Provides rear panel mounted type TNC input connector.
Option R5:	Rack mounting hardware for installation into standard 19 inch rack width.

SECTION 2

INSTALLATION AND OPERATION

SECTION 2

INSTALLATION AND OPERATION

2.1 INTRODUCTION

This section describes the various inspection, installation and operational procedures common to the Model 970 Microwave Frequency Counter.

2.2 UNPACKING AND INSPECTION

Upon receipt of the instrument from the shipper, inspect the shipping container for any external damage incurred during transit. Any indication of such damage must be noted by both the shipper and customer, and should be reported to the insurance investigator immediately.

Remove the instrument from the packing case and visually inspect it for obvious physical damage (scratches, dents, broken fittings, etc). In the event of damage, notify the factory or your nearest Eldorado representative - - DO NOT attempt to use the instrument as electrical damage may result.

Every instrument is shipped with 2 instruction manuals. Verify any specified options or modification against your purchase order. Changes or special modifications are described by a yellow addendum included at the front of the manual.

2.3 POWER REQUIREMENTS

The instrument is equipped with a standard 3 prong (NEMA) power cord that automatically grounds the instrument chassis when connected to a standard grounded power receptacle. An adapter providing an instrument ground must be used whenever termination to a bi-terminal outlet is necessitated.

The Model 970 is capable of operating from either a 115 or 230 volt ac, 50-60 Hz primary power source. The instrument is normally shipped from the factory in the 115 volt configuration. If operation from a 230 volt source is desired, follow the steps outlined in Table 2-1, 230 Volt Operation.

TABLE 2-1

230 VOLT OPERATION

STEP	ACTION
1	Slide the rear panel 115/230 switch to the position revealing the numerals 230.
2	Remove the existing 1.0 ampere SLO-BLO fuse (rear panel) and replace with a 0.5 ampere SLO-BLO type.
3	Conspicuously label the instrument for 230 volt operation.

CAUTION

The optional high stability oscillators (Options C, C1, D, D1, E and E1) are designed to operate from a specific primary power source. Under NO circumstances attempt to convert to an alternate power source when any of the oscillator options are incorporated within the instrument.

2.4 INCOMING CONFIDENCE CHECK

Prior to packaging the instrument for shipment, extensive operational, alignment and calibration checks were performed. To satisfy electrical integrity of the instrument at the receiving bench, a simple self-test procedure can be undertaken. The self-check requires no addition equipment and is intended only to verify basic operation. Prior to performing the self-check, it is recommended that the operator become familiar with the basic operating controls described in paragraphs 2.6 and 2.7. Table 2-2 outlines the self-test procedure.

TABLE 2-2

SELF-TEST

STEP	ACTION
1	With the POWER switch in the OFF position, connect the line cord to an appropriate power source.
2	Verify the proper positioning of the rear panel 115/230 volt line switch.
3	Set the rear panel TIME BASE switch to the INTernal position.
4	Set the front panel STORAGE switch to the ON position (up) and the DISPLAY control to mid-range.
5	Rotate the MODE/RANGE switch to the TEST position.
6	Rotate the POWER OFF/ON switch clockwise to the ON position.
7	The display will illuminate indicating the internal reference oscillator's output frequency (1 MHz).
8	Rotate the RESOLUTION switch through its various positions noting decimal location and display indication.

2.5 INSTALLATION

The Model 970 is operable upon receipt requiring only the connection of a suitable input

and termination of the line cord to a proper ac power source. A self locking elevating bail is attached to the front "feet" to elevate the front panel for more convenient viewing.

2.5.1 Installation Considerations

Cooling is provided by a rear panel mounted fan. The air intake duct must remain unobstructed and sufficient rear panel clearance must be maintained to assure adequate air circulation.

2.5.2 Rack Mount Installation

Installation of the Option R5 rack mounting kit is outlined in Table 2-3. All necessary hardware, with the exception of the screws securing the instrument to the rack, are supplied within the kit.

TABLE 2-3

OPTION R5 RACK MOUNT ASSEMBLY

STEP	ACTION
1	Secure a rack handle to each rack ear with the supplied hardware.
2	Remove the two sets of screws securing the side panels to the chassis. These screws may be discarded.
3	Using the supplied screws, secure the rack ears to the side panels.
4	Secure the instrument into the vacant rack cavity and complete the necessary input, output and power terminations.

2.6 FRONT PANEL DESCRIPTION

Table 2-4 and Figure 2-1 describe the front panel controls and functions.

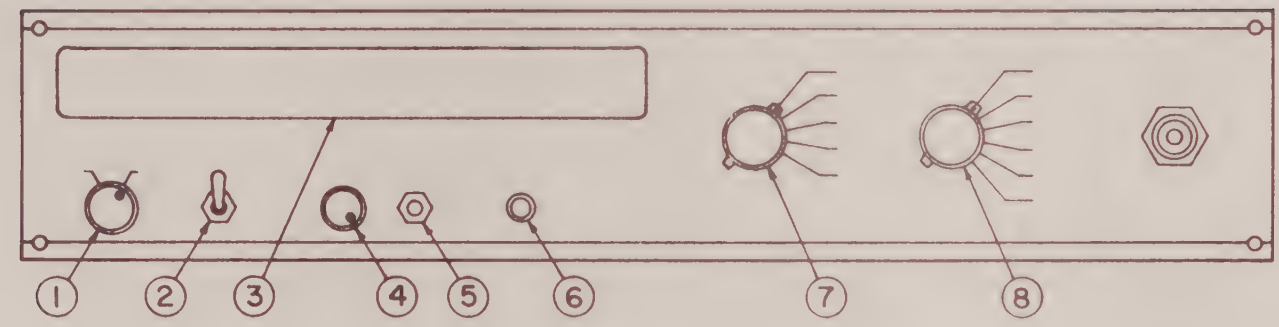


FIGURE 2-1

FRONT PANEL

TABLE 2-4

FRONT PANEL DESCRIPTION

INDEX	NOMENCLATURE	FUNCTION
(1)	POWER OFF/ON Switch	Primary power switch which supplies primary power to the instrument when rotated clockwise to the ON position. When any of the optional high stability oscillators are incorporated into the instrument, connection of the line cord to the power source supplies oven power irrespective of the POWER switch position.
(2)	STORAGE ON Switch	A toggle switch providing a storage feature (solution only) in the ON (up) position or visual display of the measurement in progress in the off (down) position.

TABLE 2-4 (Continued)

(3)	Display	Nine numerical indicator tubes with automatically positioned decimal points. In the frequency mode, the readout is in kHz as indicated by the front panel nomenclature. There are no units associated with the count mode.
(4)	DISPLAY Control	A combination potentiometer and switch controlling the display duration. The display ti time is variable from 0.1 seconds (ccw) to 10 seconds (cw) or INFinitely displayed by closing the switch contacts in the extreme clockwise direction.
(5)	RESET Pushbutton	A momentary pushbutton switch effecting instrument reset when depressed.
(6)	GATE Lamp	An indicator which illuminates during the measurement interval indicating a measurement in progress.
(7)	RESOLUTION Switch	A five position rotary switch affording the desired resolution and the determinant for decimal location. The 1.0 Hz and 0.1 Hz positions are reserved for the 20 Hz - 120 MHz range only.
(8)	MODE/RANGE	A six position rotary switch selecting one of four available modes of operation and/or the desired frequency range.
(8A)	TEST Position	Provides a self test function when selected. Instrument functions in the 20 Hz - 120 MHz frequency range measuring the 1 MHz internal oscillator's reference frequency.

TABLE 2-4 (Continued)

(8B)	COUNT ON Position	Instrument totalizes the number of cycles of input to 999999999 or until manual reset or selection of the COUNT OFF mode. Decimal point information is disabled in the COUNT mode.
(8C)	COUNT OFF Position	When selected, the COUNT OFF position disables the input storing the totalized count until reset. Counting is resumed by selecting the COUNT ON position.
(8D)	20 Hz - 120 MHz	When selected, the instrument functions as a direct frequency counter within the 20 Hz to 120 MHz range.
(8E)	110 - 700 MHz	When selected, the instrument functions as a frequency counter within the 110 to 700 MHz range.
(8F)	0.6 - 3.2 GHz Position	When selected, the instrument functions as a frequency counter within the 0.6 to 3.2 GHz range.

2.7 REAR PANEL DESCRIPTION

Table 2-5 and Figure 2-2 describe the rear panel controls and functions.

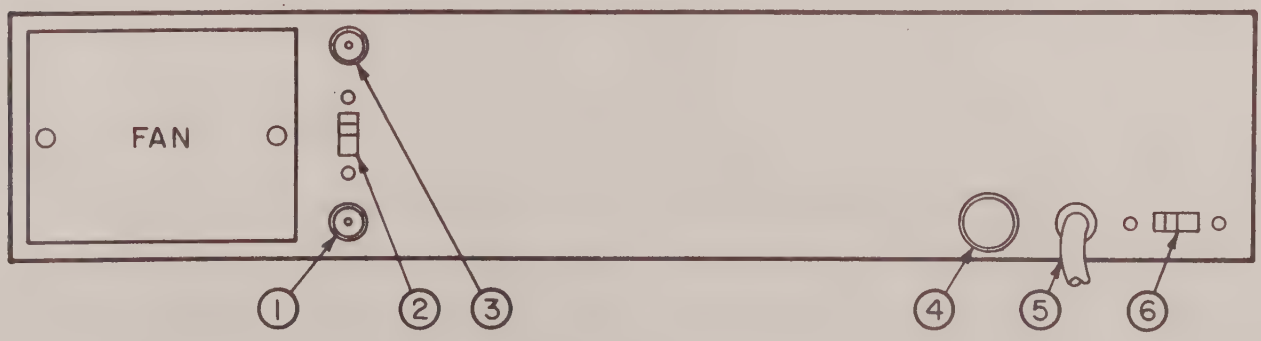


FIGURE 2-2
REAR PANEL

TABLE 2-5

REAR PANEL DESCRIPTION

INDEX	NOMENCLATURE	FUNCTION
(1)	RESET Connector	A BNC-type connector effecting remote reset when a ground is applied on the inner conductor.
(2)	INT-EXT Switch	A slide switch permitting instrument operation from the internal oscillator in the INTernal position or from an external reference in the EXTernal position.
(3)	MON/IN Connector	A BNC connector providing a means of monitoring the internal oscillator when the INT-EXT switch is in the INTernal position or the input for the external standard when the INT-EXT switch is in the EXTernal position.
(4)	1A SB Receptacle	The primary power fuse holder containing a 1 ampere SLO-BLO type fuse (115 volt operation). When operating from a 230 volt source, the fuse should be replaced with a 0.5 ampere SLO-BLO type fuse to adequately protect the instrument.
(5)	Line Cord	A six foot tri-conductor cable providing a means of supplying ac power to the instrument and terminated with a molded NEMA type male connector which automatically grounds the instrument chassis when connected to a grounded power receptacle.
(6)	115-230 Line Switch	A recessed slide switch permitting instrument operation from either a 115 or 230 volt ac source (Refer to Section 2.3).

2.8 OPERATION

The Model 970 is capable of direct frequency measurements in excess of 3 GHz and of totalizing events at up to a 120 MHz rate to 999,999,999 counts. The ensuing table outlines the basic operational procedures.

TABLE 2-6

BASIC OPERATION

STEP	ACTION
1	Connect attached cord to appropriate power source.
2	Verify correct positioning of rear panel 115/230 volt line switch.
3	Insure that the rear panel TIME BASE switch is in the INT position.
4	Rotate (cw) the POWER ON/OFF switch to the ON position and note that the display illuminates.
5	Set the DISPLAY control to mid-range.
6	Place the STORAGE switch to the ON position and place the MODE/RANGE switch to the TEST position.
7	The display will indicate the time base reference frequency (1 MHz) in kHz with decimal location determined by the selected RESOLUTION switch position. This provides a visual indication that the instrument is functioning correctly.

TABLE 2-6 (Continued)

8		To perform frequency measurements, connect suitable input (refer to the input characteristics in Table 1.1) to the front panel INPUT connector.
9		Place the MODE/RANGE switch to the corresponding range position and select the RESOLUTION switch position offering the maximum resolution. The counter will display the correct input frequency.
10		Rotate the DISPLAY control to the extreme clockwise position (INF). The display will retain the reading indefinitely until manual RESET is effected.
11		To perform totalizing measurements, select the COUNT ON position of the MODE/RANGE switch. Insure that the applied input is within listed specifications.
12		The counter will totalize (count) the number of cycles of input to 999,999,999.
13		Select the COUNT OFF position of the MODE/RANGE switch.
14		The count will stop, holding the latest count until manual reset or return to the COUNT ON position.

SECTION 3

THEORY OF OPERATION

SECTION 3

THEORY OF OPERATION

3.1 INTRODUCTION

This section describes and explains the theory of operation of the Eldorado Model 970 Frequency Counter from three increasingly detailed perspectives. The sampling technique is first discussed followed by a block diagram approach to the overall theory of operation. In conclusion, a detailed description at the circuit level is undertaken to furnish the reader with a comprehensive understanding of the individual circuits which constitute the Model 970 Frequency Counter.

3.2 SAMPLING PRINCIPLE

A sampling technique is utilized to achieve the high frequency measurements common to the Model 970. By generating an integral subharmonic of the applied input frequency and consequently solving for the harmonic multiple, the instrument is capable of realizing measurements in excess of 3 GHz. Once the harmonic number is discerned, the time base is expanded by the harmonic number while the subharmonic is counted directly by the count chain. Since the frequency of the subharmonic is counted for a duration multiplied by the harmonic number, the resulting solution is equal to the applied input frequency.

3.3 SAMPLING TECHNIQUE

The purpose of the sampling technique is to reduce the input frequency to enable ordinary counter circuits to count very high frequencies. Referring to Figure 3-1, the unknown frequency (f) is split into two equal signals and consequently directed to a "countdown" circuit and an "input sampler" circuit.

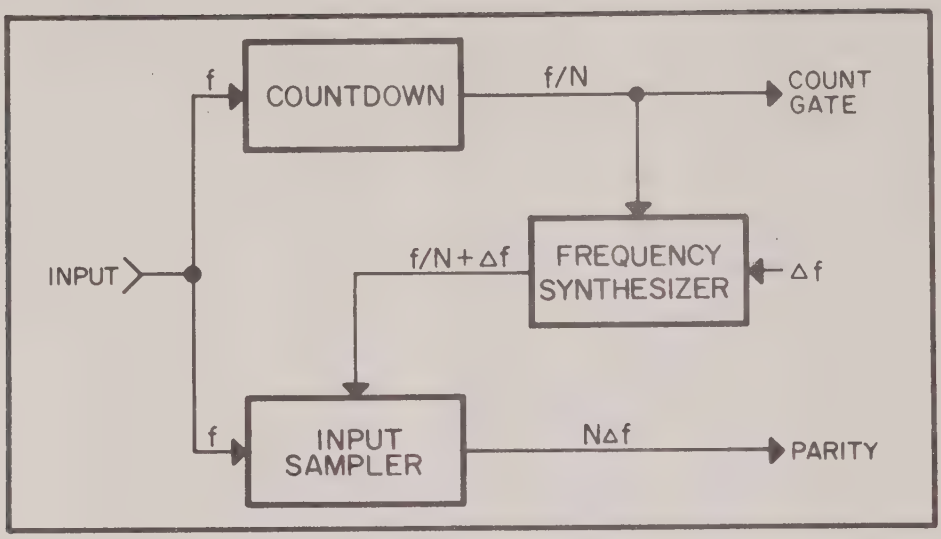


FIGURE 3-1

INPUT BLOCK DIAGRAM

The countdown circuit consists of a tunnel diode astable multivibrator. This circuit free-runs at a frequency compatible with the digital counting circuitry (below 120 MHz). An input signal higher than this natural frequency will drive the multivibrator at some integral sub-multiple of the applied input. Mathematically, the countdown circuit's output is the input frequency (f) divided by the harmonic number (N) or f/N. Figure 3-2 illustrates a hypothetical countdown output with N equal to six.

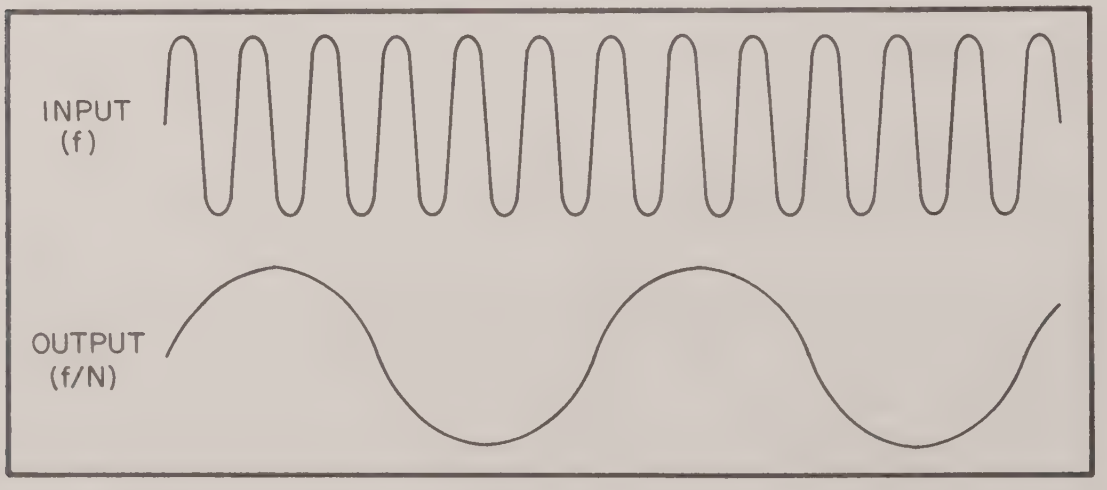


FIGURE 3-2

COUNTDOWN OUTPUT

The input sampler circuit observes (samples) the input signal for an "instant" on command. If the countdown circuit's output (f/N) were used directly to strobe the sampler, no information would be gained in the determination of the harmonic multiple. As an example, assume that the countdown circuit is syncronized to the fourth sub-multiple of the input frequency. The strobe pulses, at the countdown output's rate, occur at 1/4 the input frequency. Since the strobe pulse and the input are in phase, the sample occurs at the same point on the input waveform each time resulting in a dc level output proportional to the amplitude at the point on the input waveform at which sampling occurs (refer to Figure 3-3).

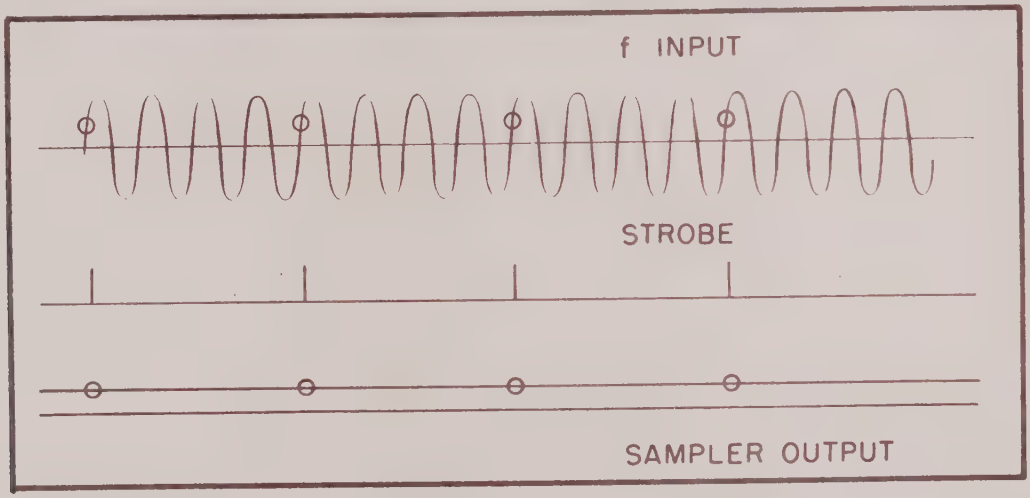


FIGURE 3-3
SAMPLER OUTPUT WITHOUT SLEWING

If the sampling frequency were "slewed", that is, each sample occuring slightly ahead or behind in time, each successive sample would coincide with different points on the input waveform. As illustrated in Figure 3-4, the sampler's output is a low frequency reproduction of the input frequency.

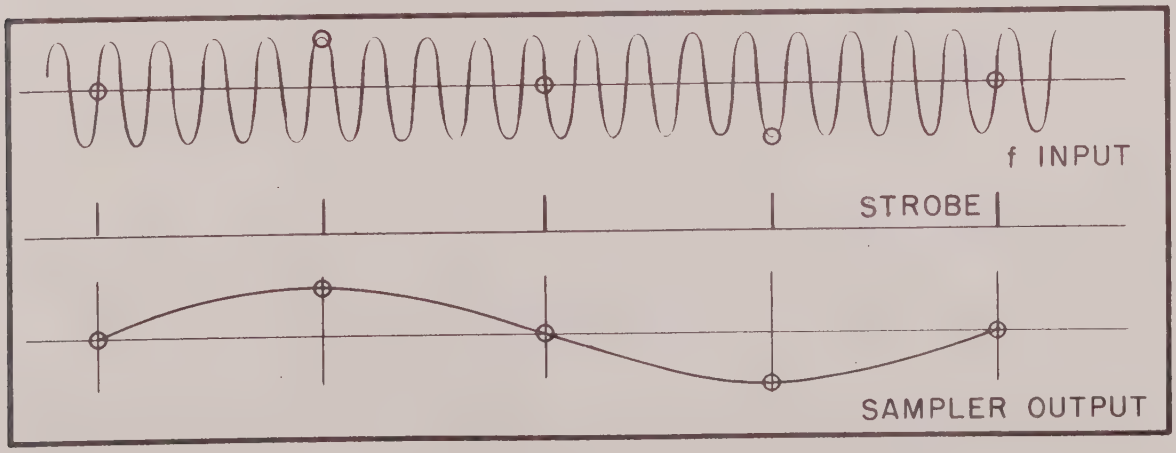


FIGURE 3-4
SAMPLER OUTPUT WITH SLEWING

To provide the necessary offset, the countdown circuit's output is first mixed with a low frequency signal within the frequency synthesizer. The synthesizer's output is the countdown circuit's output (f/N) plus the low frequency signal (Δf) or, mathematically, f/N + Δf.

The addition of f/N + Δf can be shown vectorially.

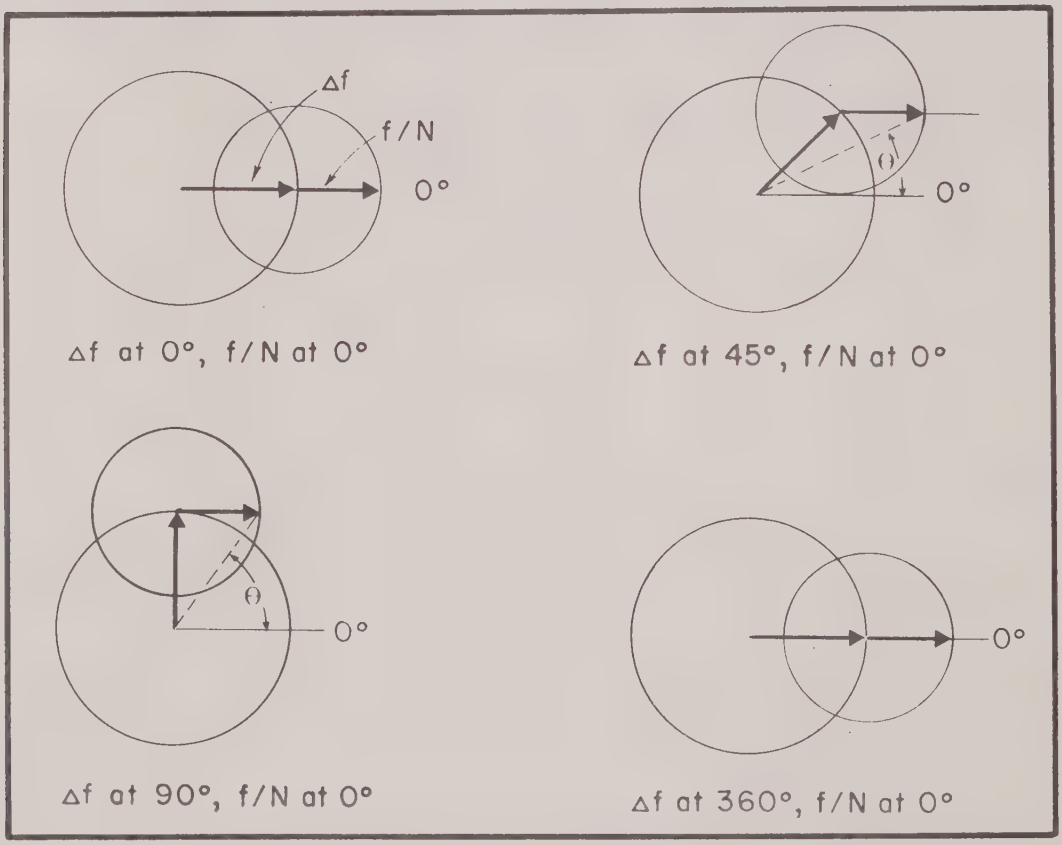


FIGURE 3-5
VECTOR ADDITION OF f/N AND Δf

The two vectors rotate in a counter clockwise direction at a rate determined by their respective frequencies. In the examples shown, the resultant (dotted vector) is shown to be a progressive phase change as the Δf vector rotates through 360°. In respect to the original 0° reference, we have progressively advanced the point of initial reference of the f/N vector through 360° as the Δf vector completes one revolution.

As an example, assume the count down circuit's output frequency to be exactly 10 megahertz (f/N = 10 MHz). The slewing frequency is 5 kilohertz (Δf = 5 kHz). In the vector representation then, the Δf vector makes 5,000 counter clockwise revolutions per second while the f/N vector completes 10,000,000 revolutions per second.

In respect to time, the Δf vector makes one complete revolution in 200 microseconds while the f/N vector completes 1 revolution in 100 nanoseconds. The resultant phase of the f/N vector changes 360° for one revolution of the Δf vector. Since 360° of the f/N vector is 100 nanoseconds, a total change of 100 nanoseconds in 200 microseconds is realized. The problem now becomes how much change occurs in the time of f/N passing the initial zero reference over a period of 100 nanoseconds of Δf if 100 nanoseconds of change occurs in one complete period of 200 microseconds of Δf? Expressed as a mathematic ratio we have:

$$\frac{\text{X change}}{100\ \text{ns}} = \frac{100\ \text{ns}}{200\ \mu\text{s}}$$

Solving for the unknown change (X) we have:

$$\text{X change} = \frac{10^{-7} \times 10^{-7}}{2 \times 10^{-4}} = \frac{10^{-14}}{2 \times 10^{-4}} = 5 \times 10^{-11} \text{ or 50 picoseconds}$$

The slewing rate per period of f/N is 50 picoseconds. Therefore each 100 nanosecond period of f/N will lose an additional 50 picoseconds. Since the f/N ± Δf signal from the synthesizer is used to strobe the input sampler, each successive sample will occur at 100 nanoseconds minus 50 picoseconds. That is, if the first sample were at 100 nanoseconds (100,000 picoseconds) the succeeding strobe pulses would occur at 100,000 -50 picoseconds or at 100000, 199950, 299900, etc, picoseconds respectively.

Referring to the vector summation, it will be noted that for one revolution of Δf, the f/N vector is advanced in phase by 360°. Since 360° is one cycle, for every cycle of Δf there will be precisely one additional cycle of f/N.

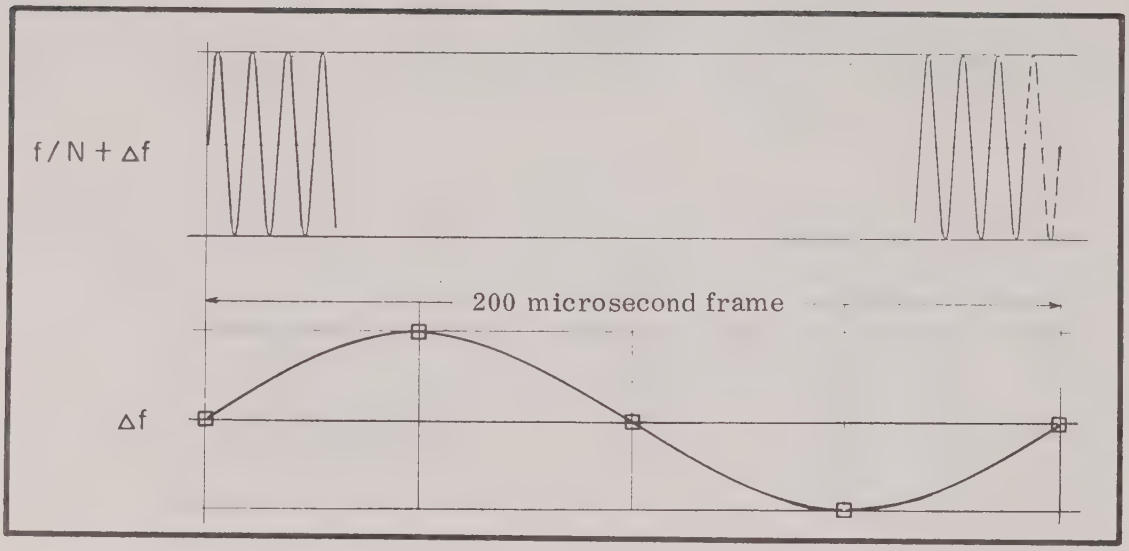


FIGURE 3-6

ADDITION OF f/N AND Δf

If f/N equals 10 megahertz, 2,000 cycles will occur in a 200 microsecond frame of one cycle of Δf. Since the vector addition of f/N and Δf adds one additional cycle of f/N, 2,001 cycles of f/N + Δf occur within the frame.

This corresponds to a time per cycle of f/N of:

$$100 \text{ nanoseconds} \left(\frac{2000}{2001}\right) \text{ or } 99.950024038 \text{ nanoseconds.}$$

The slew rate (change in time per cycle) is therefore approximately 100 nanoseconds - 99.9500 nanoseconds = 0.050 nanoseconds or 50 picoseconds or exactly $50\left(\frac{2000}{2001}\right)$ picoseconds per cycle.

To obtain a solution for the value of N a hypothetical case of an input frequency (f) of 500 MHz and a countdown output (f/N) of 10 MHz with a 5 kHz slewing frequency (Δf) and corresponding slew time of 50 picoseconds will be employed as an example.

The period of a 500 megahertz signal is 2 nanoseconds. In a 200 microsecond frame, 100,000 cycles of f will occur. Similarily, 2,000 cycles of f/N will occur and, since we

add precisely one cycle of f/N with Δf, 2,001 cycles of f/N + Δf will occur. Since f/N + Δf performs the storbing of the input, 2001 sampling strobes will be performed. The sampling slewing rate is 50 picoseconds per cycle. In order to progress entirely over and sample an entire cycle of the input frequency (f), which has a period of 2 nanoseconds (2000 picoseconds), forty strobes must be performed.

2000 picoseconds ÷ 50 picoseconds = 40 (strobes)

In other words, one low frequency replica of the input will be generated after 40 samples. In a time frame of 200 microseconds where a total of 2001 strobes occur; 2001 ÷ 40 cycles of the reproduced input will occur; or 50.025 cycles.

The solution obtained is slightly high because of the approximation of the slew time at 50 picoseconds. Since the actual slew time is $50\left(\frac{2000}{2001}\right)$ picoseconds, the solution is in error by the factor $\left(\frac{2000}{2001}\right)$. The correct solution would be $50.025\left(\frac{2000}{2001}\right)$ or 50.000 cycles

The sampler's output is the cycles (harmonic multiple) of N per cycle of Δf. The counter derives the value of N from the expression N Δf by counting the sampler's output for one period of Δf.

3.4 BLOCK DIAGRAM ANALYSIS

This section explains the theory of operation from a functional block diagram. All circuits and their respective functions are covered to present an overall understanding of the basic instrument and to complement the detailed circuit description outlined in Section 3.5.

3.4.1 Input Power Divider

The input signal is cabled directly from the INPUT connector to the input power divider where it is divided into two equal signals and consequently cabled to both the countdown and input sampler circuitry. A small amount of the input signal energy is tapped and cabled directly to the 120 MHz DCU for low band (20 Hz - 120 MHz) applications.

3.4.2 Countdown Circuit

The countdown circuit accepts the high frequency output from the input power divider and, in turn, generates a low frequency sub-multiple (f/N) of the applied input frequency (f). The generation of the sub-multiple is accomplished by one of two astable tunnel diode multivibrators incorporated into the countdown circuitry. In the mid band (110 - 700 MHz), a multivibrator with a natural frequency between 8.75 and 9.75 MHz is enabled while in the high band (0.6 - 3.2 GHz) a multivibrator with a natural frequency range of 32 to 37 MHz is enabled. The resonant frequency of the multivibrators is determined by the dc level output from the ramp generator. When not tuned near an integral sub-harmonic of the applied input, "error reset" signals step the ramp generator until an approximate sub-multiple is encountered.

When the frequency of the enabled multivibrator is sufficiently close to an integral sub-harmonic, the influence of the applied input signal causes a "phase lock" condition which holds the multivibrator at a stable sub-harmonic.

The output from each multivibrator is routed through a low pass filter network to remove any high frequency complements, amplified and transformer matched before being coupled to both the frequency synthesizer and 120 MHz DCU. Figure 3-7 illustrates the functional block diagram for the countdown circuit.

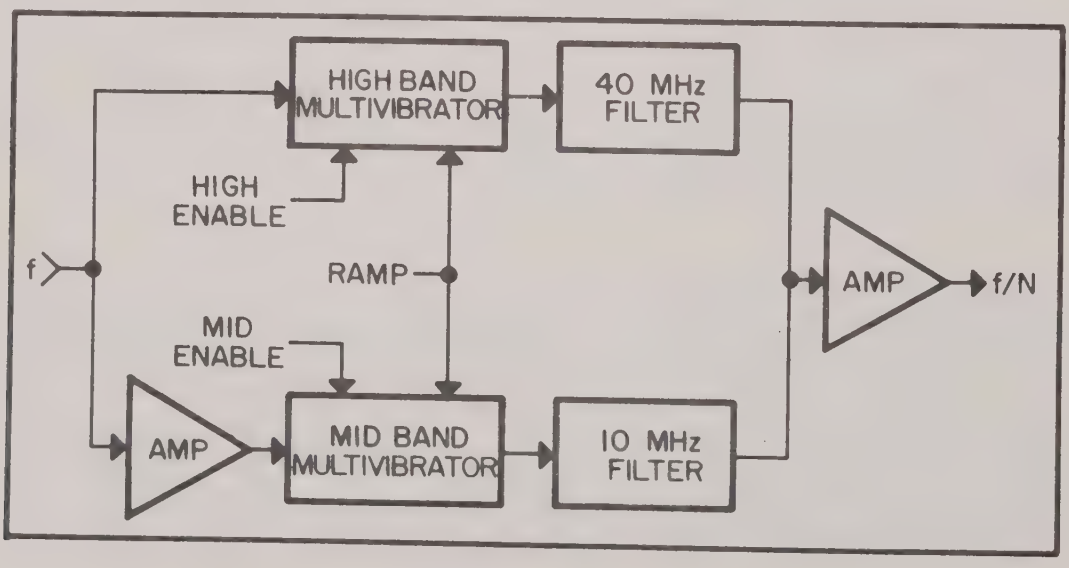


FIGURE 3-7

COUNTDOWN CIRCUIT BLOCK DIAGRAM

3.4.3 Frequency Synthesizer Circuit

The frequency synthesizer circuit provides slewing for the sampler circuit by combining the countdown circuit's output (f/N) with the 5 kHz signal (Δf) from the phase shifter. During operation employing the high band (0.6 - 3.2 GHz), the synthesizer also provides a divide-by-four function to reduce the output frequency to within the range of the sampler circuit.

The synthesizer utilizes two RF phase shift networks, one tuned to approximately 9 MHz (mid band) and the other to approximately 36 MHz (high band), to divide the input signal (f/N) into two identical signals with a 90° phase shift.

A pair of balanced modulators accept the two phase shifted signals from the band selected phase shift network. One of the 5 kHz signals (Δf) from the phase shifter is routed to one of the balanced modulators while the other 5 kHz signal (90° out of phase) is routed to the other balanced modulator. The consequent mixing of the two signals within the modulator results in a double side band output of f/N $\pm\Delta$f from each modulator. The combining of the two outputs, since they are out of phase, results in a single sideband output of either f/N + Δf or f/N - Δf.

NOTE: While the sign of the slewing frequency does not alter instrument operation, the manual will refer to the slewing frequency as f/N + Δf to maintain clarity.

In the mid band, the single sideband (SSB) output (f/N + Δf) is first filtered, amplified and then coupled to the sampler circuit by an auto transformer. In the high band, the SSB output is filtered, squared for logic level compatibility, divided-by-four by a pair of TTL flip-flops and then routed through the same filter, amplifier and auto transformer common to the mid band.

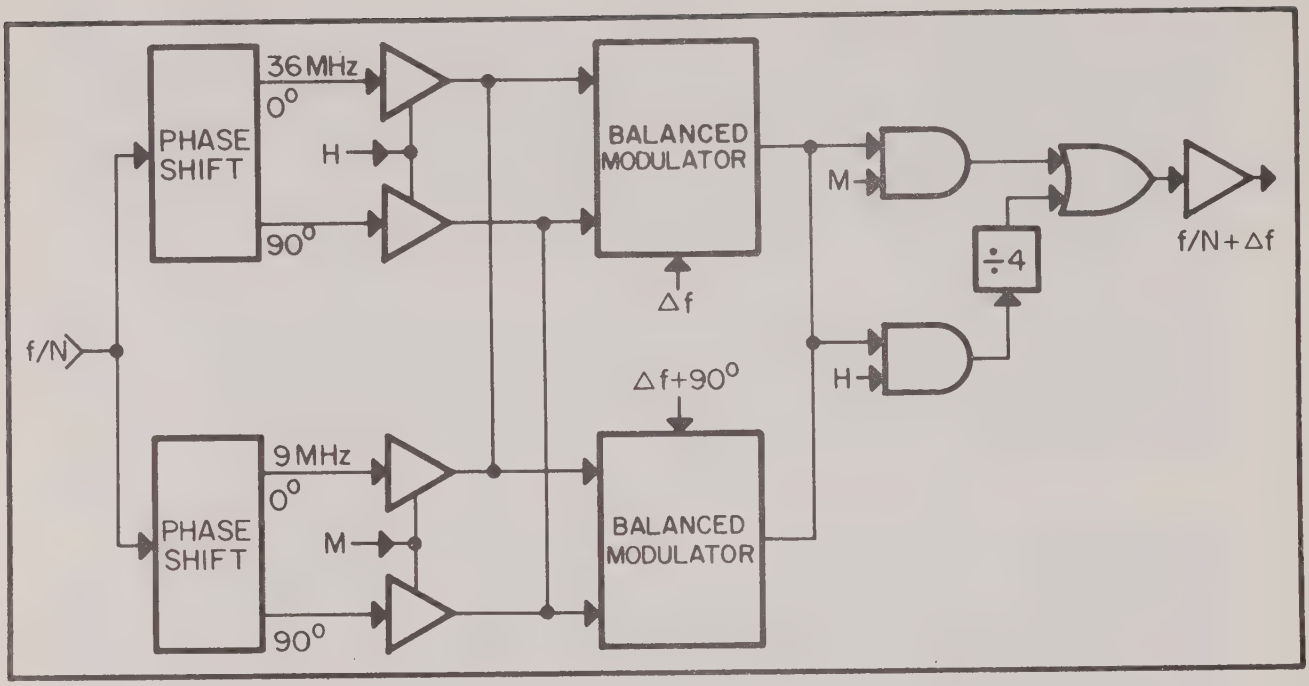


FIGURE 3-8

FREQUENCY SYNTHESIZER
BLOCK DIAGRAM

3.4.4 Sampler Circuit

The sampler circuit accepts two separate inputs; the high frequency input (f) from the power divider and the slewing input ($f/N + \Delta f$ or $f/4N + \Delta f/4$) from the synthesizer circuit.

The high frequency input is coupled to a diode sampling gate while the slewing input from the synthesizer is amplified and shaped into a string of extremely fast pulses (typically 200 picoseconds). These pulses are used to open (strobe) the sampling gate thereby coupling a fraction of a cycle of the input signal to the gate of a FET source follower.

The FET output is filtered to remove the carrier (8-10 MHz). The resultant series of positive and negative pulses (rough sinewave) with a normal frequency between 40 and 500 kHz is amplified, clipped, squared and coupled to the parity circuit as the $N\Delta f$ signal.

The amplitude of the NΔf sinewave decreases sharply as the input frequency increases. At the lower frequencies, the sampling pulse (approximately 200 picoseconds in duration) is considerably shorter than the period of the input signal and, is generally, totally positive or negative for the full duration of the pulse. However, at the higher frequencies, the sampling pulse width approaches the input period exhibiting a nulling effect resulting in a reduced output amplitude. A compensation network is incorporated into the amplifier stage to offset this high frequency inefficiency.

In the mid band (110 - 700 MHz), the amplifier gain is increased which, conversely, decreases the signal-to-noise ratio. This aids in the prevention of "locking on" to a false harmonic due to the higher amplitude signals characteristic of the lower frequencies.

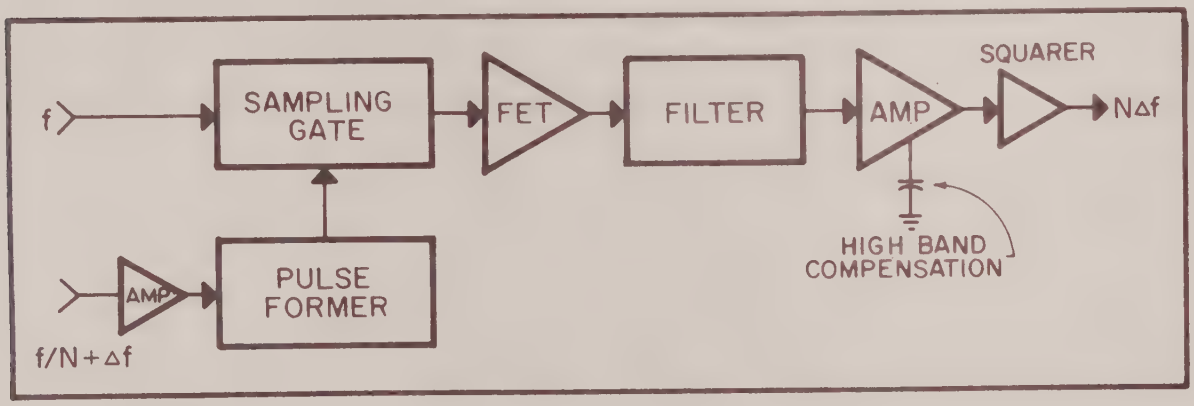


FIGURE 3-9

SAMPLER BLOCK DIAGRAM

3.4.5 Phase Shifter Circuit

The phase shifter circuit accepts the 5 kHz square wave from the time base circuitry and generates two 5 kHz sinewaves (separated by 90° phase shift) to the balanced modulators of the frequency synthesizer circuit.

The 5 kHz square wave is converted into a rough sinewave by RC circuits and coupled directly into the input of an operational amplifier. The feedback components form a highly selective "twin T notch filter" which attenuates all higher and lower

frequency components resulting in a 5 kHz sinewave of extremely low harmonic distrotion. This output is the 0° phase or "sine" output. A voltage divider taps a portion of this output which is applied to a second operational amplifier, the output of which is shifted in phase by 90° (cosine output).

3.4.6 Error Counter Circuit

The error counter circuit is a six bit binary counter, the contents of which are increased by one for each "error reset" signal generated by the parity circuitry. No provision for resetting the binary is included and, on overflow, its contents simply return to zero. The initial state of the error counter is of no consequence as successive error reset signals will advance the counter to its appropriate state corresponding to the applied input and harmonic multiple.

3.4.7 Ramp Generator Circuit

The ramp generator circuit is an electronically switched voltage divider which generates an analog voltage output proportional to the contents of the error counter. Two flip-flops and a divide-by-sixteen circuit provide 64 voltage "steps" which determine the resonnant frequency of the countdown circuit's multivibrators.

3.4.8 Parity Circuit

When enabled by the time base circuitry, the parity circuit counts the $N\Delta f$ signal from the sampler for a period of Δf. The resultant tentative value of N is stored into the N counter circuitry and compared with successive values of N. If a deviation in the ensuing value of N is detected, an error reset signal is generated. This signal, in turn, resets the control logic and count chain circuitry as well as advancing the error counter which steps the ramp generator.

If the parity circuit completes four successive N consistency checks without encountering an error, the count gate is enabled and a frequency measurement is initiated. While the instrument is attempting a measurement, a fine parity circuit monitors the countdown frequency for instability. The fine parity circuit ignores the first error but will interrupt the measurement interval and generate an error reset signal upon receipt of the second fine parity error indication.

The main parity circuit performs the following tests for the value N:

1. The quantity 2N must be even. This check eliminates the possibility of a ± one count error in the N counter.
2. The value N must be equal to or greater than eight as a harmonic multiple of less than eight is possible only outside of the specified frequency bands.
3. The least significant digit of four successive values of N must be equal. This check greatly reduces the possibility of "locking on" to a false sub-harmonic.

The NΔf signal from the sampler circuit is coupled to the input of the flip-flop designated "2N" (refer to Figure 3-10). A 200 microsecond signal from the time base is coupled to the input of the "2N Gate" flip-flop. The output from the 2N Gate (divided-by-two) is used to enable the "2N" flip-flop for 400 microseconds of each 1 millisecond frame. Since 400 microseconds is equal to two periods of Δf, 2 times N pulses appear at the input. The output from the 2N flip-flop is one half the input (divide-by-two) or N with a possible one count gating error.

If the output from the 2N flip-flop is in the "1" state at the conclusion of the 400 microsecond count interval, the quantity 2 times N is considered odd. This output is coupled to the main parity gate (three-input NOR gate) where it will effect an error reset.

The output of the 2N flip-flop (quantity N) is loaded into both the N counter (Section 3.4.10) and the parity counter. The parity counter is a one-decade BCD register which only counts the least significant digit of the value N. Immediately after the quantity N is loaded into the N counter, a flip-flop referred to as "N Lockout" is set by the time base. This disables the N count line denying subsequent values of N to the N counter circuitry.

The value of the least significant decade of the N counter and the contents of the parity counter are compared by a set of "exclusive OR" gates (XOR). The first comparison is obviously true as both the N counter and parity counter are loaded by the same quantity N output from the 2N flip-flop.

The second "burst of N" from the 2N flip-flop, is denyed from the N counter by the N lockout flip-flop and is therefore only counted by the parity counter. The exclusive OR gates (XOR) compare the contents of the N counter with the updated parity counter. Any discrepancy between the two counters will cause the eventual generation of an error reset signal by the action of the main parity gate.

The third input to the main parity gate is the "N must be greater than 8" function. The "over 8" flip-flop is set by the N counter when the value of N exceeds the integral 8. After each "burst of N" (at the conclusion of each 1 millisecond time frame) the main parity gate is interrogated by the time base. If any of the three parity errors are present ($N \neq N_1$, $N < 8$ or $2N$ is odd), an error reset signal is generated advancing the error counter and ramp generator and initiating a new measurement. A subsequent value of N is counted by both the N and parity counters and the parity function is repeated.

If four successive N parity checks are valid (four 1 millisecond time frames), the parity circuit, after 800 microseconds, releases the time base hold off flip-flop. This represents a total time of 9.8 milliseconds as the time base was preset to 5 milliseconds. The release of the time base holdoff allows the time base to advance and enables the control logic initiating a measurement.

During the measurement interval, fine parity circuitry checks the stability of the sampler output. The fine parity counter counts the least significant digit of the $N\Delta f$ signal for 8 milliseconds (forty times the period of Δf). If the value of N is an integral, 40N will be divisible by ten and the count decade should be clear at the end of the 8 millisecond interval. Since the binary "1" bit is not employed, a one count error is tolerable.

At the end of each 8 millisecond period, the contents of the fine parity counter are interrogated. A "2", "4" or "8" bit will set the fine parity error 1 flip-flop. A second error will clear the fine parity error 1 flip-flop and, in turn, set the fine parity error 2 flip-flop producing an error reset signal, initiating a new measurement.

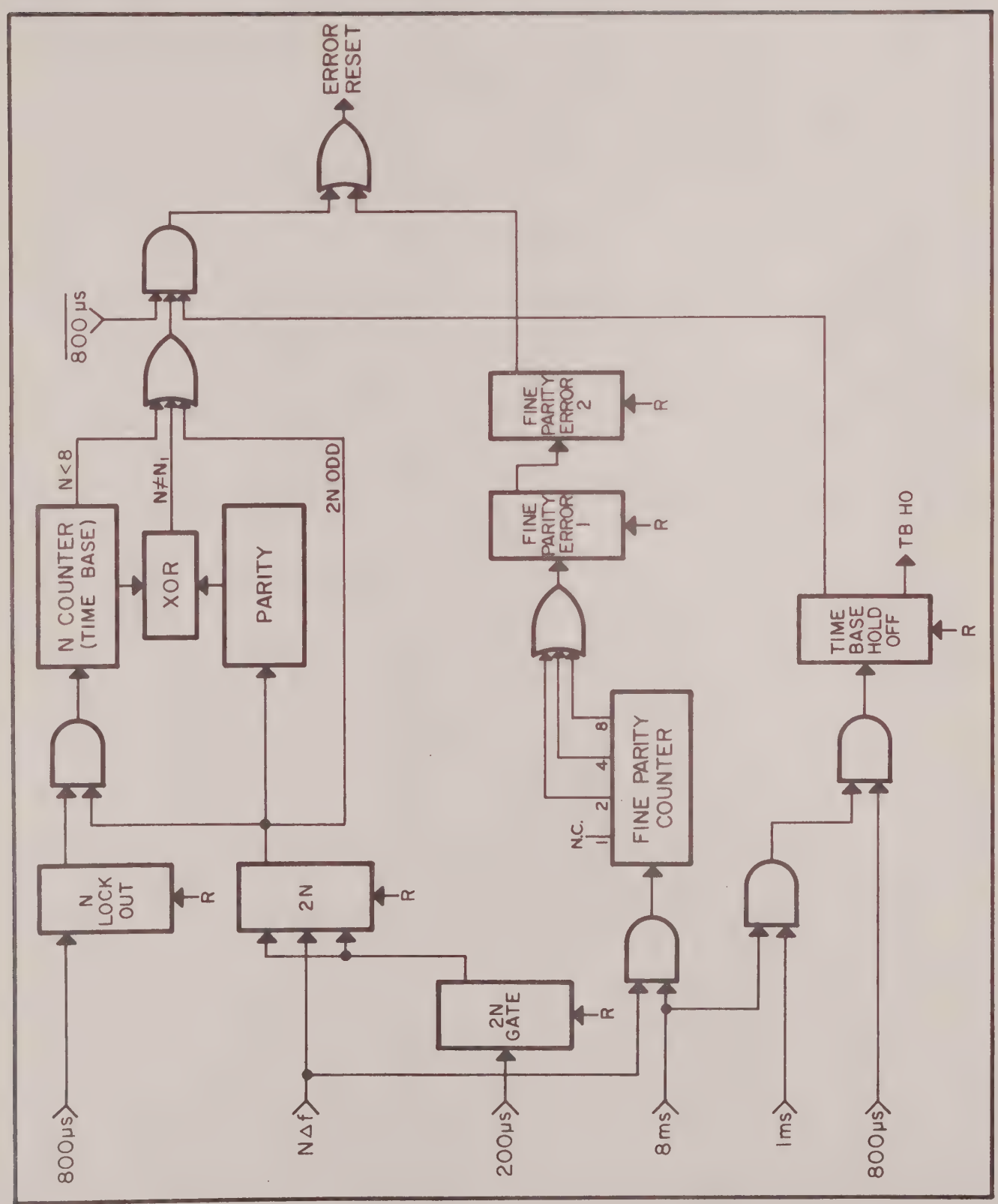


FIGURE 3-10

PARITY BLOCK DIAGRAM

3.4.9 Time Base Circuit

The time base circuit is referenced to an internal 1 MHz crystal oscillator. From this 1 MHz signal, the time base derives the timing signals required by both the parity and control circuitry. Basically, the time base circuit consists of an overlapping string of decade dividers with their corresponding reset and preset circuits and a series of gates to enable and disable the control logic (refer to the Time Base Block Diagram, Figure 3-11).

A string of four decade dividers provide the parity circuit timing signals. The 500 kHz output signal from the first decade is used to load the time base multiplier from the N counter in the mid and high frequency bands. The 100 kHz output from the first decade is used to clear the TB output flip-flop immediately after it is set by the selected time base pulse. The third decade provides the 5 kHz square wave employed by the phase shifter circuit, the 200 and 800 microsecond signals used by the parity circuit and a 1 kHz output signal to the following decade.

The fourth decade is initially set to 5 milliseconds by the preset pulse. Its outputs (1 ms and 8 ms) are employed by the parity logic to release the time base holdoff flip-flop after a total elapsed time of 9.8 milliseconds, initiating a measurement.

The 1 kHz output from the third decade is used to drive a series of four decade dividers. This chain provides gate times of 1 ms, 10 ms, 100 ms, 1 s and 10 s as selected by the corresponding RESOLUTION switch position.

In the mid and high bands, the 1 and 10 second gate times are not employed and the decades, now free of their timing functions, serve as the time base multiplier. When enabled by the control circuitry, via the N flip-flop gate, the 500 kHz signal drives the N counter and the 1 second decade simultaneously. Since the N counter has been previously loaded with the value N, the 500 kHz signal adds to the value of N until the counter overflows (99 counts) and the 500 kHz signal is disabled. The 1 and 10 second decades, cleared by the first time base pulse, will contain the complement of N or 100-N.

The time base output (a selected period in the low band or a multiplied selected period in the mid and high bands) sets the "time base output" flip-flop. This flip-flop is cleared by the 100 kHz output signal within the time base. The clearing of the flip-flop, not its setting, triggers the control logic.

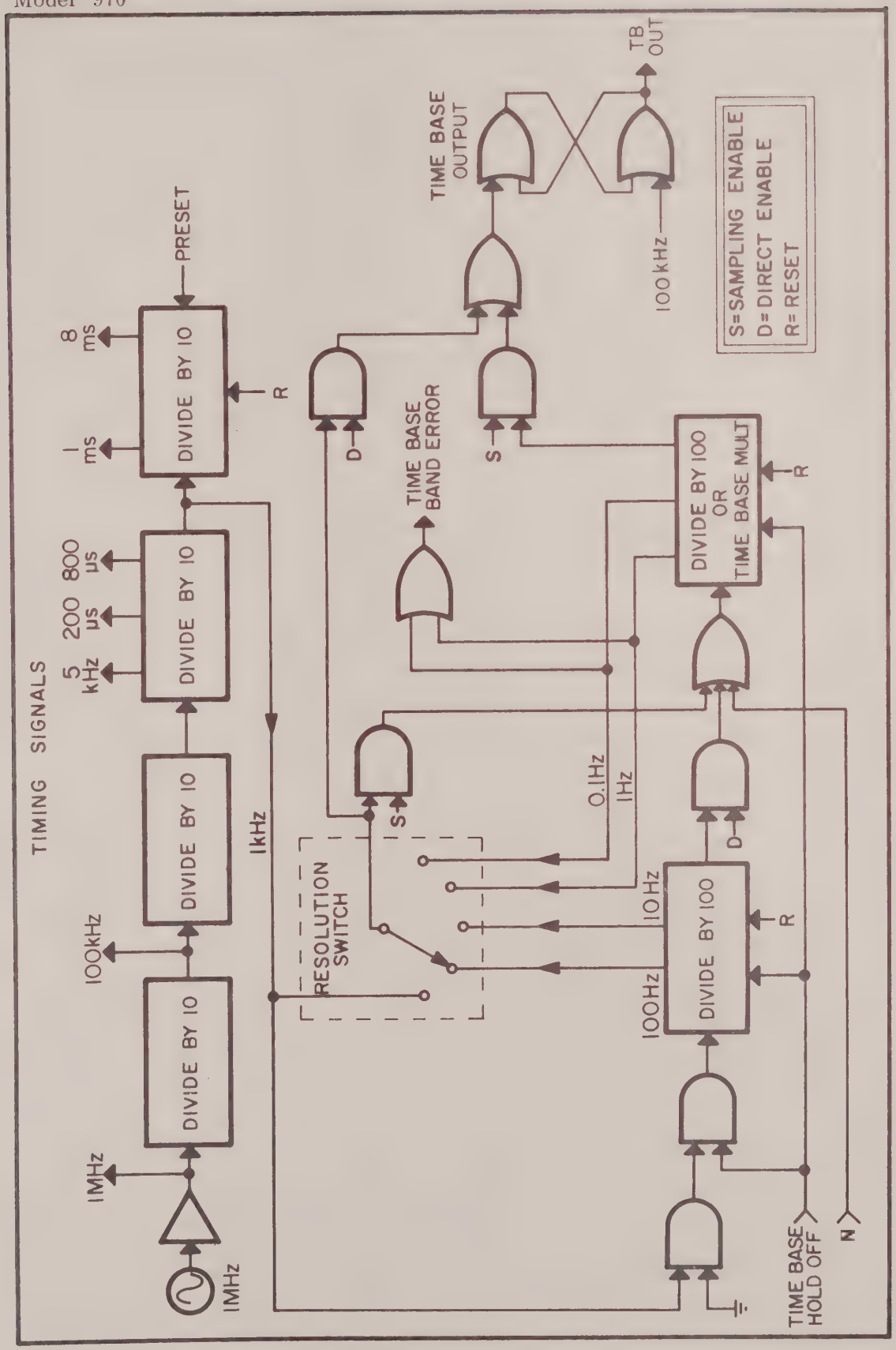


FIGURE 3-11
TIME BASE BLOCK DIAGRAM

3.4.10 N Counter

The N counter is a two-decade BCD counter that stores the value of N before transferring it to the time base multiplier.

The N counter is loaded with a tentative value of N by the parity circuit. If parity accepts the value, it releases the time base holdoff flip-flop, enabling the time base circuitry. This enables the control logic, which, in turn, sets the start-stop flip-flop and enables the N flip-flop gate. When enabled, the N flip-flop gate passes the 500 kHz time base signal to the N counter and time base multiplier as described in the previous section.

3.4.11 Reset and Control Circuit

The reset and control circuit controls the count gate and generates the reset and preset signals on command from the time base or parity circuitry.

The transition of the time base output flip-flop to its zero state sets the start/stop flip-flop, opening the count gate (120 MHz DCU) and illuminating the front panel GATE lamp. The ensuing transition of the time base output flip-flop clears the start/stop flip-flop, closing the count gate thereby stopping the count, and setting the display flip-flop. The display flip-flop, in turn, enables the storage, reset and preset circuitry.

The output of the display flip-flop triggers a "one-shot" multivibrator which generates the storage-transfer pulse. This pulse transfers the accumulated count from the storage registers into the decoder circuits enabling the numerical indicator tubes. The setting of the display flip-flop also initiates the display interval by enabling the timing capacitors to charge to the conduction level of a unijunction transistor. The "firing" of the unijunction sets a flip-flop which, in turn, generates the reset and MECL reset pulses. These pulses clear the count chain, time base, reset and control and parity circuits. The trailing edge of the reset pulse generates the preset pulse which presets the time base to 5 ms.

The generation of an error reset signal from the parity circuit will simultaneously enable both the reset and storage-transfer circuits. This action causes the display to indicate all zeros thereby avoiding an erroneous reading.

3.4.12 120 MHz DCU

The 120 MHz DCU (decimal counting unit) is, in truth, the least significant digit of the count chain. Since it is geographically distant from the remainder of the count chain, employs an exclusive family of logic, and includes an important control function, the 120 MHz DCU will be discussed separately.

The 120 MHz DCU includes an input amplifier, the count gate, a decade of MECL high-speed logic and MODE/RANGE switch logic. It accepts input signals from the direct input amplifier, the countdown circuit and the 1 MHz test signal from the time base. In the low band and COUNT modes, the input signal is amplified and squared. The amplifier is dc coupled with a dc feedback loop.

The MODE/RANGE switch logic enables either the output from the input amplifier, the countdown circuit output or the 1 MHz test signal from the time base to the count gate, the instrument's primary control gate. The time base circuit enables the count gate for a fixed time interval, allowing the DCU to operate. The output from the DCU is buffered and routed to the succeeding DCU in the count chain.

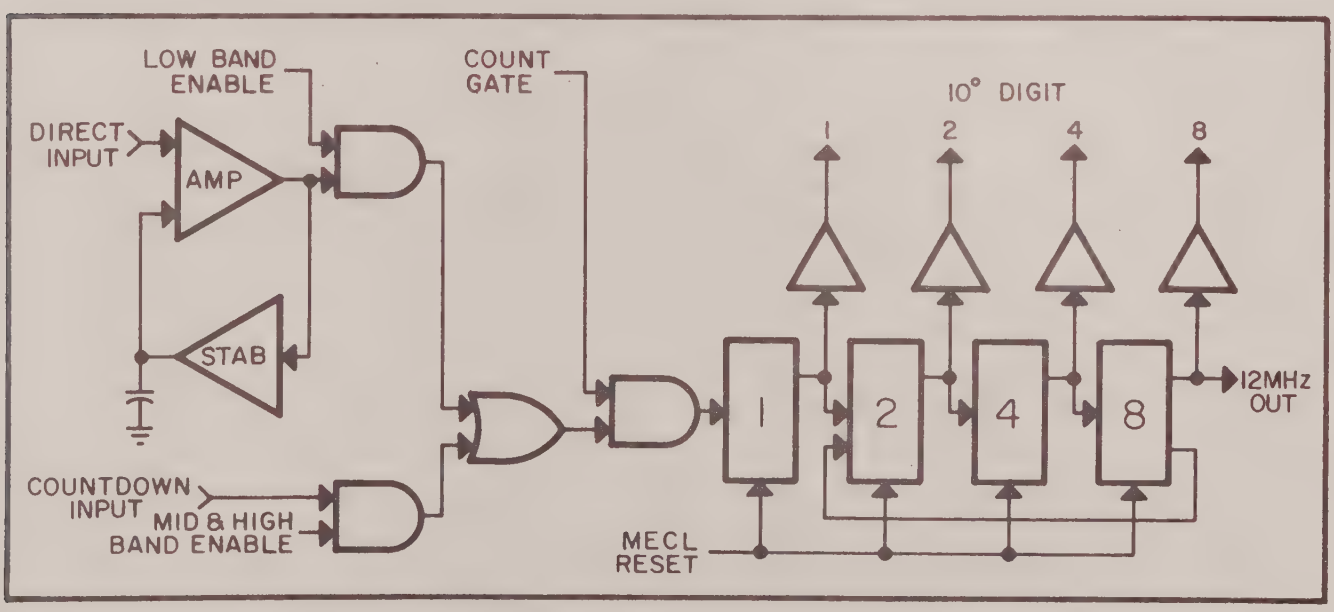


FIGURE 3-12
120 MHz DCU BLOCK DIAGRAM

3.4.13 Count Chain

The count chain consists of the remaining DCUs with their corresponding decimal indicator tubes. Each DCU is comprised of a decade counter, storage register and decimal decoder circuit. Each decade counter provides a 1-2-4-8 BCD count to its corresponding storage register and a divide-by-ten output to the succeeding decade counter. The 1-2-4-8 BCD output and the "12 MHz" carry signal from the 120 MHz DCU are directly coupled to the count chain. The storage register and decimal decoder circuits associated with the 120 MHz DCU are incorporated into the count chain's circuitry.

The count chain consists of nine full digits and will be advanced by either the direct or countdown input until the count gate is disabled by the reset and control circuitry. The ensuing storage transfer pulse transfers the accumulated count from the storage registers to the decimal decoders which, in turn, enable the individual digits within the display indicator tubes. Since the storage transfer pulse occurs after the count gate is disabled, the display will read only the correct solution or all zeros (parity error indication).

3.4.14 Power Supplies

The instrument derives its regulated and unregulated dc levels from either a 115 or 230 volt ac, 50-60 Hz source. Table 3-1 lists the various levels and their circuit applications.

TABLE 3-1

POWER LEVELS

VOLTAGE	APPLICATION
+230Vdc (unregulated)	Numerical indicator tube plate voltage.
+12Vdc (regulated)	High level logic.
-12Vdc (regulated)	High level logic.
+3.6Vdc (regulated)	RTL logic.
+4.5Vdc (regulated)	DTL and TTL logic.
-5.2Vdc (regulated)	MECL logic.

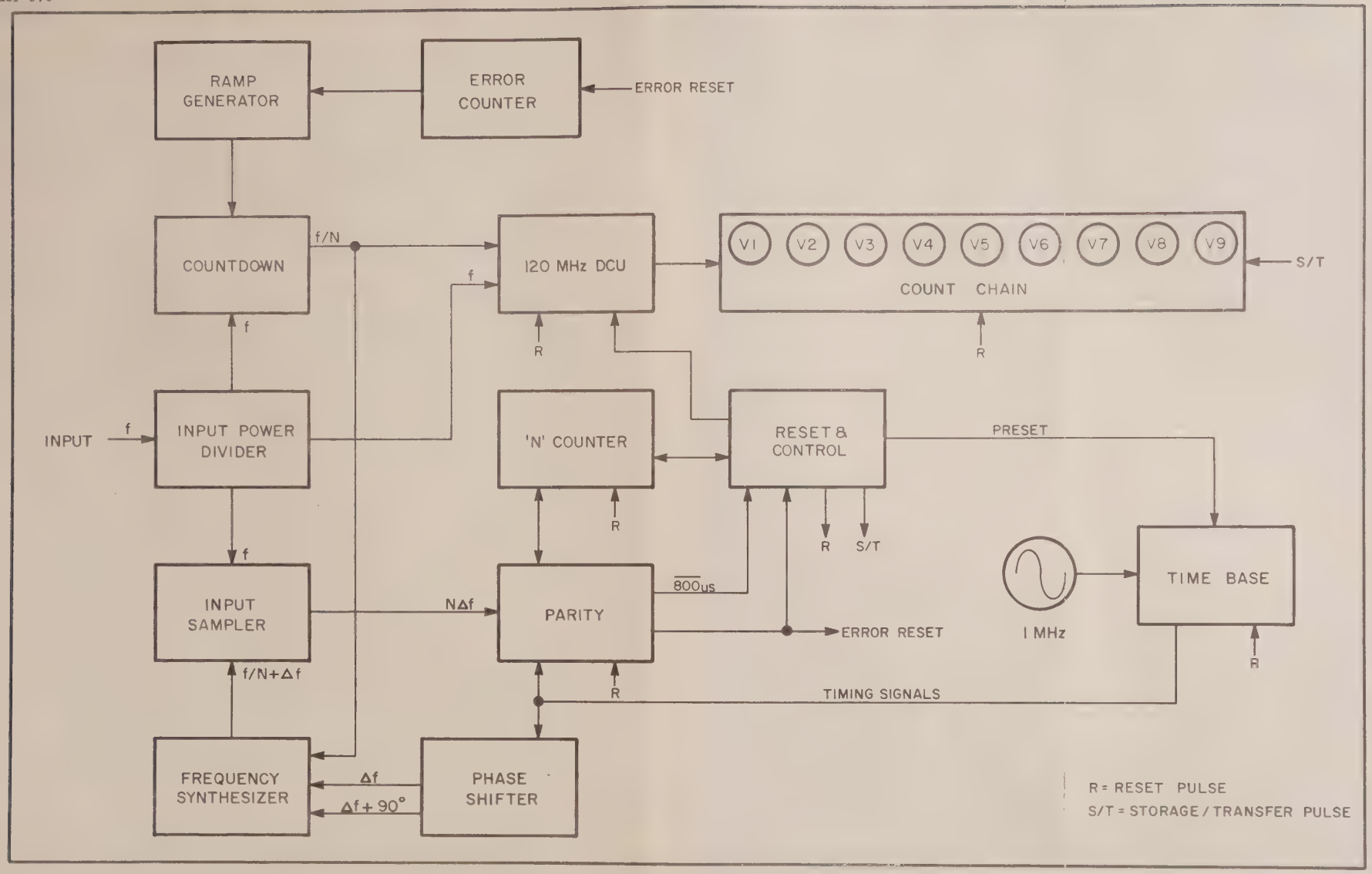


FIGURE 3-13
SIMPLIFIED BLOCK DIAGRAM

3.5 DETAILED THEORY OF OPERATION

This section approaches the theory of operation from a detailed circuit description. Subsection numbering is consistant with the block diagram analysis of Section 3.4. The drawing number included in the subsection title block refers to individual schematic diagrams included within Section 5 of this manual.

3.5.1 Input Power Divider (C-11-06052)

The applied input signal is cabled directly from the INPUT connector to J101, the input power divider input. Two pairs of 100Ω resistors split the input signal into two equal signals which are routed to the countdown and input sampler circuits from connectors J102 and J103. R103 couples a small fraction of the input power to the base of Q101, the driver transistor to the 120 MHz DCU for low band applications. C101 attenuates input frequencies above 300 MHz to aid in preventing spurious oscillations.

3.5.2 Countdown Circuit (C-11-06414)

The countdown circuit includes an input amplifier, two tunnel-diode multivibrators, two low-pass filters, an output amplifier, and the switching and biasing circuits.

The input (from J102 on the mother board, the output of the power divider) is loaded to about 50 ohms by R1, R37, C1, and the base-emitter junction of Q1. Q1, the mid band input amplifier, is in a grounded-base configuration. Note that it is a metal-case transistor with an internal shield and that its case and shield are soldered as directly as possible to the circuit board's ground plane.

The output of Q1 is coupled through an attenuator and RF choke (L1, a zig-zag etch on the PC board) to CR1, the mid-band multivibrator tunnel diode. CR5, the high band TD, is driven directly by the divider R1/R37.

The MODE/RANGE switch applies +12V to R18 and CR3 in the mid band, R32 and CR8 in the high band, and neither in the low (direct) band. In either sampling band, the selected multivibrator will run freely.

The two multivibrators are similar. The discussion will center around the high-band multivibrator (CR5), but the parallel components on the mid band circuit will be called out in parentheses.

Zener diode CR8 (CR3) applies 6.8V to the resistor string R31-28-27 (R15-13-12). The idling voltage at R27 (R12), and thus the TD bias current, is adjustable by R31 (R15). Current flows through the inductors L7 and L6 (L2 and L3) till CR5 (CR1) "fires", that is, goes into its high-voltage state. This voltage step decreases the current through the coils and after a time the tunnel diode turns off again. CR5 oscillates at about 35 MHz and CR1 at 9 MHz. The output of the ramp generator (the analog output of the error counter) is led to the multivibrators through R23 and CR6 (R5, CR2). As the voltage increases, so does the dc bias current through the tunnel diode, and so does the frequency of the oscillator. CR5 is adjustable from about 33 to 36 MHz and CR1 from about 8 to 10 MHz.

A small amount of energy from the input signal is coupled to the tunnel diode through C21 (C6). If the natural frequency of the multivibrator is sufficiently close to some subharmonic of the input frequency, the input signal will provide enough "kick" to the tunnel diode to synchronize the multivibrator to that frequency. The error counter increases the ramp voltage till synchronization occurs.

The physical placement of the components discussed thus far is critical. Note particularly the mounting of the high-band components (CR5 et. al.). These components should be left alone as much as possible.

L1, L6, and L7 are not "coils" in the most obvious sense but zig-zag lines of etch on the printed circuit card. They do, in fact, act as inductors, not delays. It is interesting to note that when the current through the printed inductors changes direction, the field in the inductor changes path as well as direction.

The output of the multivibrators is buffered by emitter follower Q5 (Q2) and passed through a 40 MHz (10 MHz) low-pass filter to eliminate any leftover energy from the input signal. It is amplified by Q6 (Q3) and Q4 and coupled to the output cable by autotransformer T1. CR4 and CR7 are used as -0.7V voltage sources to set the switching levels of Q3 and Q6 near ground.

The 50 ohm output cable provides an approximate 2V p-p signal to the synthesizer board. R34 and R35 provide about a 1V p-p signal to the 120 MHz DCU. C28 filters out any remaining UHF noise.

3.5.3 Frequency Synthesizer (C-11-05821)

The Frequency Synthesizer includes two pairs of RF phase shift networks, two balanced modulators, two low-pass filters, two TTL flip-flops, an output amplifier, and control circuits.

The output of the countdown board (8-10 MHz in the mid band, 30-40 MHz in the high band) is cabled to the input transformers T1 and T5. The transformer outputs are phase shifted by a pair of RC networks. The networks C1/R1 and C2/C3/R2 provide two outputs separated in phase by 90° at frequencies in the 8-10 MHz range. C2, a mica trimmer, provide fine adjustment of the phase separation. The two RF signals are amplified by Darlington buffers Q1/Q2 and Q3/Q4. The similar circuits associated with T5 provide phase shifting and amplification between 30-40 MHz.

In the mid band, the emitter resistors of Q1-4 are returned to +12V, and the inverters enabled. In the high band, transistors Q7-10 are similarly enabled. The outputs of the "wrong" phase shift networks are ignored, and the selected outputs fed to T2 and T6.

T2, T3, and CR1-4 are a "balanced modulator". Its inputs are RF from the buffer (f/N) and an AF input, Δf, through R11. Its output includes two basic components, $f/N+\Delta f$ and $f/N-\Delta f$. Note that no f/N component appears in the output.

T6, T7, and CR7-10 are a similar balanced modulator. Its inputs are similar to those of the T2/T3 modulator but separated from them in each case by 90°. The outputs of the two are connected together. The signal phases work out so that one set of side bands cancels and the other reinforces, leaving only $f/N+\Delta f$ or $f/N-\Delta f$ at the output (junction of CR5 and CR13).

R43 is the CARRIER BALANCE adjustment. It compensates for any differences in the balanced modulators.

In the mid band, +12V is applied to R12, opening gate CR5/CR6 and feeding the 8-10 MHz +5 kHz slewed countdown output to the 10 MHz low-pass filter L1-4/C9-13. This filter eliminates any harmonics and noise that may have been generated by the modulators and shapes the signal into something approaching a sine wave. The signal is amplified by Q5 and Q6 and coupled to the output through the toroidal autotransformer T4. The output is cabled to the sampler board.

In the high band, gate CR5/CR6 is disabled and gate CR13 enabled through R30. The 30-40 MHz + 5 kHz output of the balanced modulator is fed through 40 MHz low-pass filter L5-7/C28-31 to eliminate harmonics and amplified and squared by Q11-13. TTL flip-flops MC1A and MC1B divide the signal by four. The resultant output ($f/N+\Delta f/4$, or $f/4N+1.25$ kHz) is attenuated by R31 and R32. Gate CR12 CR11, enabled through R29, passes the 7.5-10 MHz signal to the 10 MHz filter and the output amplifier.

Zener diode CR14 is biased through CR5 in the mid band and CR13 in the high band. The positive dc level across it back biases the remaining gate diode (CR13 or CR5) to steer the signal through the proper filter. R38 and CR15 provide +5.1V for the TTL logic.

3.5.4 Input Sampler (C-11-05823)

The sampler accepts the input signal (0.1-3 GHz) from the power divider and the 7.5-10 MHz output of the synthesizer. It produces an output equal to $N\Delta f$. The high-frequency input is coupled to J1, loaded to 50Ω by R1-4, and coupled to the sampling gate CR1-4. Normally, this gate is back biased through R7 and R11.

The slewed countdown output is fed to P2 and amplified and shaped by Q6, Q7, and Q8. C24 is a differentiator. Its output is a series of positive and negative pulses less than 0.2 ns wide. The output (emitter) of Q8 is coupled through balancing transformer T1 and transmission line C35/L8/L9 to C28 and C29. L8 and L9 are the leads of C35, trimmed to 1.1" and bent in a semicircle. The placement of the leads is critical. R47 and R50 terminate the line properly. R49 adjusts the bias current through Q8. Step recovery diode CR13 speeds the rise time of the pulse. The positive pulses are coupled to the sampling bridge through C28 and C29. Each time the bridge is opened the FET Q1 observes a fraction of a cycle of the input wave. This sampled signal is source and emitter followed by Q1 and Q2 respectively. The 5 MHz filter C5/L1/C6 filters out the 10 MHz "carrier" frequency, leaving a signal output of 40-450 kHz, the N f frequency. The amplitude of the 40-450 kHz sinewave decreases sharply with increasing frequency. Note that at the lower sampling frequencies the 200 ps sampling pulse is considerably shorter than the input period - the sampled signal is likely to be positive or negative for the full duration of the pulse. At the highest frequencies acceptable, around 3 GHz, the pulse is nearly as long as a complete cycle of the input. Each sampling pulse transmits very little energy. Since the pulses appear at more or less constant rate (7.5-10 MHz) the amplitude of the output wave decreases as the sampling efficiency goes down.

The N f signal is amplified by Q3, Q4, and Q5. C10 boosts the gain of Q3 for frequencies above 100 kHz. C14 and C17 boost the gain of Q4 and Q5 at frequencies above 200 kHz and 400 kHz respectively. The amplified output is clipped by CR5-7 and fed to output amplifier MC1.

In mid band, CR8 is turned on through R37. The emitter of Q4 is bypassed to ground through C19, increasing the gain and decreasing the signal-to-noise ratio of the amplifier. This combats a tendency of the countdown circuit to lock on false harmonics of the input frequency in the mid band by allowing the relative noise level on the signal to increase. This makes it more likely that the parity circuits will detect the error.

MC1A amplifies the output signal and MC1B and C square it. R37 is a positive feedback loop to speed the switching time of MC1B/C. R34 and R33 fix the gain of MC1A to about 4. The output is buffered by MC1F and G and fed to the parity circuit.

3.5.5 Phase Shift Networks (B-11-06045)

The 5 kHz square-wave output of the time base is fed to the mother board and buffered by Q106. The RC circuits R114/C103 and R115/C104 knock the corners from the square wave, and R116 couples the coarse sine wave to the input of operational amplifier MC102B.

R117, R118, R119, R120, C105, C106, and C107 form a negative feedback loop around the operational amplifier. All the components save R117 are connected in a "twin-T" configuration tuned to 5 kHz. The "twin-T" circuit exhibits a very high impedance at its center frequency and a low impedance at other frequencies - it is a selective high-Q filter.

The signal input to the operational amplifier is a distorted 5 kHz sinewave, rich in high-order harmonics. The twin-T feedback loop turns the op amp into a selective amplifier, effectively filtering out the non-5 kHz components of the input and producing a clean, high-level sine wave at the output of voltage divider R121/R122. R124 and C108-110 provide high-frequency roll off for the amplifier, suppressing any tendency for it to oscillate.

MC108A is a voltage-time integrator, whose time constant is determined by R125 and C111. It shifts the phase of its 5 kHz input by 90°, and couples the shifted signal out through the divider R128/R129. R126, R127, and C112 suppress any high-order harmonics of 5 kHz that may have leaked through. MC102A is fitted with the same sort of high-frequency rolloff as MC102B. The phase-shifted 5 kHz outputs are fed to the synthesizer.

3.5.6 Error Counter (C-11-06046)

The six-bit error counter includes two integrated circuits, MC103 and MC104. MC103 is a dual J-K flip-flop connected as a straight binary counter. MC104 is a four-bit binary counter driven by the output of MC103B.

The error counter does not count errors in the truest sense of the word, because it does not necessarily start counting at zero and the number of ERROR RESET signals accepted by the counter cannot be determined by observing its contents. It rather advances once for each error received. When it fills, it clears to zero on the next ER RS and starts over.

3.5.7 Ramp Generator (C-11-06046)

The switching transistors in the ramp generator's digital-to-analog converter are not independent components but parts of RCA type CA3046 integrated circuits. Each IC contains three uncommitted transistors and one emitter-coupled transistor pair. Their mounting affords compactness and temperature stability. One half of each emitter-coupled pair is used simply as an input diode. The third uncommitted transistor in each circuit is not used.

R158 and R159 are a voltage divider providing about +1V at a low source impedance (c. 40Ω). This voltage is bussed to the bases of the D-A switching transistors. The emitter of each transistor is connected to -12V through a 10k resistor. Any transistor allowed to turn on will be a current sink of approximately 12 mA. Each emitter is also connected through a diode (or diode-connected transistor) to a flip-flop in the error counter. Any given transistor is turned on when and only when its associated flip-flop is in the zero state. Note that each diode and base emitter junction form a gate whose node will be at the higher of its two input levels.

The precision resistor ladder R135-R145 forms a voltage divider with R160. The resistance of the ladder network, and therefore the output voltage of the divider, is proportional to the weighted sum of its inputs. Each turned-off transistor adds to the output voltage. "Weighted" in this sense means "given importance according to its binary weight", that is to say, each transistor will have twice as much effect on the output voltage as the transistor to its left, ignoring the exponential feedback mentioned below. If Q105C changes the voltage by V, Q105D (two stages down the ladder) will change it by 4V.

This output is isolated from its load by the Darlington emitter follower Q105/Q104. Part of the output energy is coupled back to the emitters of the switching transistors, where they change the response of the converter from linear to inverse exponential.

The exponential wave shape allows more voltage steps in the most critical region of the countdown oscillator's voltage response than would a linear ramp, increasing the reliability and decreasing the search time of the instrument in the high band.

3.5.8 Parity Circuit (C-11-06049)

The parity circuit is negative in nature. That is, it detects errors rather than correct readings. If an error occurs, the parity circuit will stop the measurement, reset the instrument and advance the ramp generator for the ensuing measurement. When satisfied that the measurement is correct, the parity circuit merely refrains from generating an error reset signal.

The output of the sampler is a square wave from about 40 to 500 kHz (N f). This signal is coupled to the clock input of MC55B, a flip-flop referred to as 2N. The S and C inputs of the flip-flop are enabled or disabled by MC55A, and 2N GATE flip-flop. 2N GATE is set for 400 ms out of every millisecond (refer continually to the timing diagram in the last section) by the 200 μs output of the time base, acting through MC62D. This enables 2N to count 2N input pulses, and cycle N times. Its output goes to MC51B, the main parity gate. MC51B is an OR gate, whose output is defined as true when any of three possible errors occur. One of the errors is true if, at the end of a 400 ms burst, the 2N flip-flop is in the 1 state. Since 2N was originally in the "0" state and was toggled 2N times, its winding up in the "1" state implies that 2N is an odd number, which implies that N is not an integer.

Meanwhile, MC54A and B, the N LOCKOUT flip-flop is set by the trailing edge of the 800 μs pulse thru C15. This pulse occurs after one complete "burst" of N pulses has come from the 2N flip-flop. The output of the 2N flip-flop (the "burst of N") is inverted by MC54D and counted by MC53, the parity counter. This is a CμL decade, which at the end of the burst will retain the least significant decimal digit of the value of N. MC54C is enabled while N LOCKOUT is in the zero state, so that only the first burst of N is counted by the N counter. MC52 is a quadruple exclusive OR (XOR) gate, connected to compare each bit of the parity counter (MC53) with the corresponding bit of the least significant decade of the N counter. Each output of the parity gate is true if and only if the bits it compares are dissimilar. The four outputs are ORed together by MC51A

(output low for any error), inverted by MC50C, and ORed with the other possible error signals by MC51B, the main error gate described earlier.

The first burst of N is loaded simultaneously into the parity counter and the N counter. The values in the counters are tautologically equal (unless the circuitry is defective), so the bank of XOR gates detects no error. Then the N LOCKOUT flip-flop is set. The next burst-of-N counts into the parity counter (which has since been reset - see below) only, since MC54C is inhibited, disconnecting the input of the N counter.

After each burst-of-N, the 800 μs signal from the time base clears the 2N flip-flop and the parity counter thru C14 and Q12 and opens MC50D for a short time thru MC44B and RC network C16/R46. MC50D then observes the output of the parity gate.

The parity gate has yet one more input. MC49C and D comprise the OVER 8 flip-flop, an R-S flip-flop set by the 8 output of the N counter and later cleared by RESET. If the N counter has ever accepted fewer than eight input pulses - that is, N is less than 8, the count is rejected as spurious.

A fourth input of the gate, TB BAND ERROR, prevents sampling measurements (mid and high bands) when the 1 or 10 second time base is incorrectly selected. The output of the parity gate is gated with 800 μs and ORed with the output of the fine parity gate at MC50B. Any error reading causes a RESET pulse which advances the error counter, clears the control logic, and resets the time base to somewhere near zero. Then the whole merry chase through parity starts again at the beginning.

If the time base manages to count to 9.8 ms without detecting an error, MC44 sets the TB HOLDOFF flip-flop, MC47C and D, and clears the fine parity counter MC46 through a separate RC network. This occurs 4.8 ms after the start of the count, after four parity checks (the time base starts counting at 5 ms). The buffered output of TB HOLD-OFF releases the time base and allows the count to start.

Even as the count is progressing, the fine parity circuitry is checking for fresh errors. MC46, the fine parity decade counter, is allowed to count the sampler output for 8 ms (forty periods of Δf) by gate MC45C. CR3, 4, and 5 check the contents of the register. Their output is true (low) if and only if the quantity in the decade is zero or one. The zero detector is ANDed with the TB HOLDOFF signal by MC47B, inverted by MC47A,

ANDed with the 9 ms timing signal from MC44A thru C20 and MC49B, and fed to the flip-flops MC48B and A, called FP ER 1 and FP ER 2. The first time the quantity 40N (that has overflown the fine parity decade) is not divisible by ten (or divisible by ten with a remainder of one) MC48B is set. The second error clears MC48B, setting MC48A. MC48A's output is gated with the 800 μs signal from the time base by MC49A, whose output is ORed with the error reset circuitry. The second error discovered by the fine parity thus fires ER RS, resets the counter, destroys whatever was accumulating in the count chain, advances the error counter (and the ramp) and initiates a new measurement.

3.5.9 Time Base (D-11-06044)

The time base circuit is responsible for the generation of the various timing signals employed by the parity circuit and for the establishment of the measurement interval for which the count gate is enabled. The circuit is referenced to a 1 MHz crystal oscillator and incorporates a string of decades and related logic to perform its various functions. The time base circuitry also includes the N counter and the time base multiplier circuits.

The time base circuit is referenced to a temperature-compensated 1 MHz crystal oscillator. Energy from the emitter of Q1 is fed back to its base through R2 and the ac voltage divider C4/C5, driving Y1 into oscillation. Trimmer capacitor C1 is used to adjust the oscillator output frequency to precisely 1 MHz and C2 compensates for variation with temperature. The output of the oscillator is buffered by emitter follower Q2 and coupled through C7 and R6 to inverters MC62A and MC62B. R7 provides positive feedback to increase the switching time, squaring the signal, which is, in turn, directly coupled to the input of decade counter MC61.

The output of MC61 (100 kHz) is coupled to the input of decade counter MC60 and to inverter MC62C. The inverted 100 kHz signal from MC62C is used to clear the TB output flip-flop, MC70A and MC70B. Decade counter MC60 provides a divide-by-ten function resulting in a 10 kHz signal at the input of MC58.

Decade MC58 provides the 200 μs and 800 μs timing signals used by the parity circuit, the 5 kHz signal (Δf) used by the phase shifter circuit and the 1 kHz signal which is coupled to the succeeding decade MC57 and, via gates MC56C and MC56B to decade MC69. Decade MC57 provides the 1 ms and 8 ms timing signals used by the parity circuit. Initially, decade MC57 is preset to 5 ms (1 ms and 4 ms) by the preset pulse from the reset and control circuit.

The setting of the TB holdoff flip-flop (parity circuit) after 9.8 ms produces a low state on the TB HO lead which enables the time base to the remaining decade dividers by reverse biasing transistor Q3. MC69, the 10 ms decade, is preset to 8 as long as the TB holdoff flip-flop is clear. The remaining three decades (MC63, MC68 and MC68) are each preset to 9 when the TB holdoff flip-flop is clear. The presetting of these four decades, via MC64 and MC73, enables the frequency measurement to start approximately 1 ms after parity accepts a tentative value of N. Decades MC63, MC67 and MC68 provide timing periods of 100 ms, 1 s and 10 s respectively. The 1 and 10 second decades are used only during low band applications and serve as the time base multiplier in the sampling bands. The selected time base is determined by the RESOLUTION switch position resulting in a low state on one of the emitter leads of transistors Q5 through Q9. A low state will enable one of the NOR gates associated with the selected time base (MC65A, MC65C, MC65B, MC72A or MC72C).

During low band operation (20 Hz - 120 MHz), the low state from the MODE/RANGE switch on the low band enable lead enables NOR gates MC71C and MC56A while causing the output of NOR gate MC70D to assume a high state. The high state output from MC70D disables the error reset function on the control and reset circuit, the 500 kHz signal to the N counter at NOR gate MC59D, the 5 kHz Δf signal to the phase shifter circuit at NOR gate MC59A while enabling the time base from MC56A to the 1 and 10 second decades (MC67 and MC68) through 4-input NOR gate MC66B. Recalling that the 10 ms decade (MC69) was preset to 8 and that the remaining decades were preset to 9, when the TB holdoff flip-flop is set (after 9.8 ms), the 1 ms time base pulse from NOR gate MC56B will be counted by MC69. The next pulse will overflow decades MC69, MC63, MC67 and MC68.

The positive transition of the selected time base pulse (100 ms, 1 s or 10 s) will be inverted by its corresponding NOR gate (MC65B, MC72A or MC72C) and inverted again through MC66B to the input of enabled NOR gate MC71C. The low state output from MC71C is directly coupled to enabled NOR gate MC71A producing a high state output which, coupled through capacitor C8, will set the TB output flip-flop comprised of MC70A and MC70B. The TB output flip-flop will be cleared almost immediately by the inverted 100 kHz timing signal from decade MC61 through inverter MC62C. The clearing of the TB output flip-flop will set the start-stop flip-flop on the reset and control circuit enabling the count gate. The next positive transition of the time base pulse will again set the TB output flip-flop which will, in turn, be cleared by the 100 kHz time base signal.

The start-stop flip-flop will be toggled to its low state disabling the count gate and sto stopping the count.

During mid or high band operation, the low band enable signal is in its high state causing the output of MC70D to be low. The low state output enables the error reset function from the parity circuit on the reset and control circuit, the 5 kHz Δf signal to the synthesizer at NOR gate MC59A and the 500 kHz time base signal to the N counter through MC59D.

The negative transition of the selected time base (1 ms, 10 ms, or 100 ms) will be inverted by its corresponding NOR gate (MC65A, MC65C or MC65B) inverted again through either MC66B or MC71B to enabled NOR gate MC65D. The high state output from MC65D is coupled to the input of 4 input NOR gate MC66B adding 1 count to decade MC67. Decades MC67 and MC68, originally preset to 99 by the initial setting of the TB hold-off flip-flop, both overflow causing the 8 bit output of MC68 to assume a high state.

The high state output is coupled through R22 to enabled NOR gate MC71D. The low state output from MC71D is, in turn, inverter by enabled NOR gate MC71A, setting the TB output flip-flop through C8. The clearing of the TB output flip-flop by the 100 kHz time base signal sets the start-stop flip-flop on the reset and control circuit enabling the count gate.

The setting of the start-stop flip-flop produces a low state on the N F/F gate lead at pin 5. The low state from the TEST/NORMAL switch (NORMAL position) produces a high state output from MC74A which, coupled across capacitor C10, clears the flip-flop comprised of MC74C and MC74B enabling the 500 kHz signal at NOR gate MC70C. Recalling that the N counter (decades MC76 and MC75) was previously loaded with N counts from the parity circuit, the enabled 500 kHz signal will be added to the existing count until the decade overflows, resetting the flip-flop (MC74C and MC74B). The 500 kHz signal, while being added to the N counter, is simultaneously enabled to decade MC67 through 4-input NOR gate MC66B. Since these decades were cleared by the first time base pulse, they will contain the complement of N or 100-N counts when the 500 kHz signal is disabled.

The filling of the time base multiplier (decades MC67 and MC68) will be completed prior to the receipt of the negative transition of the next time base pulse since counting is accomplished at a 500 kHz rate.

The ensuing time base pulses will be counted by the "time base multiplier" until N counts are obtained and the decades overflow. On overflow, the 8 bit from MC68 assumes a high state output which, as previously described, sets the TB output flip-flop through C8. The clearing of the TB flip-flop by the 100 kHz time base signal toggles the start-stop flip-flop to its low state disabling the count gate.

3.5.10 N Counter (D-11-06044)

The N counter is a two decade counter comprised of MC76 and MC75, incorporated into the time base circuitry. As described, the N counter is loaded with the first tentative value of N by the parity circuit. The 1, 2, 4 and 8 bits of the least significant digit (MC76) are coupled to the exclusive OR (XOR) gates within the parity circuit where subsequent values of N are compared. The N count from the parity circuit is coupled to NOR gate MC74D. Since, at this time, the flip-flop comprised of MC74C and MC74B is set, the N count will be enabled through NOR gate MC74D, inverted by Q10 and coupled to the input of the first count decade. The N >8 parity function is also associated with the N counter. The 8 bit of the least significant decade is coupled to the base of transistor Q11. Since the 8 bit will be in its high state until the count of 8, transistor Q11 will be forward biased holding the N >8 leading to the N >8 flip-flop low, maintaining its initial set position. On the count of 8, the 8 bit assumes a low state which will reverse bias transistor Q11, enabling the positive potential at its collector which, in turn, will clear the N >8 flip-flop.

After parity releases the TB holdoff flip-flop and the start-stop flip-flop is set by the time base, the 500 kHz signal will be added to the N count until decade MC75 overflows resetting the flip-flop (MC74C and MC74B), disabling the 500 kHz signal to the N counter and time base multiplier.

3.5.11 Reset and Control (D-11-06543)

The reset and control circuitry opens and closes the count gate on command from the time base circuit and is responsible for the generation of the storage-transfer, reset, MECL reset and preset pulses employed throughout the instrument.

The setting of the TB holdoff flip-flop at reset clears start-stop flip-flop MC43A and display flip-flop MC43B through inverter MC42A. These flip-flops are enabled when parity releases the TB holdoff after 9.8 ms. The clearing of the TB output flip-flop by the 100 kHz timing signal after its initial setting by the selected time base pulse will

toggle the Q output of MC43A to its low state and the $\overline{Q}$ output to its high state. The low state Q output enables the N F/F gate on the time base circuit (mid and high band operation) while the high state $\overline{Q}$ output back biases Q13 enabling the count gate on the 120 MHz DCU. Holding Q13 off forward biases Q14 which, in turn, forward biases Q15 illuminating the front panel GATE lamp indicating a measurement in progress.

The next cycle of the TB output flip-flop will toggle the start-stop flip-flop's Q output to its high state disabling the N F/F gate and its $\overline{Q}$ output to its low state disabling the count gate, extinguishing the GATE lamp and toggling display flip-flop MC43B. The Q output from MC43B will be low disabling the J and K inputs of MC43A. The high state $\overline{Q}$ output from the display flip-flop (MC43B) performs three separate functions. It disables the fine parity circuit, triggers the storage-transfer one-shot and initiates the display interval.

The Q output is coupled directly to the C input of the fine parity error 2 flip-flop, disabling fine parity gate MC49A of the parity circuit.

At NOR gate MC41D, the high state Q output from the display flip-flop produces a low state output which is coupled across C35 to inverter MC42F. Inverter MC42D provides yet another inversion driving the high level storage-transfer line to its low state, creating the storage-transfer pulse. The duration of the pulse is determined by the RC time constant of C35 and R83 (typically 15 μs).

At transistor Q19, the high state Q output forward biases the transistor driving the collector positive. This potential will discharge capacitors C37 and C38 as long as the INFinite switch contacts are closed. The discharge time is determined by the RC time constant (C37, C38 and the DISPLAY potentiometer setting) and range from approximately 100 ms to 10 s. When the FAST/NORM switch is placed in the FAST position, capacitor C36 is removed from the circuit decreasing the display time range to between 1 ms and 100 ms. Q20, the unijunction transistor, will "fire" when the charge across the capacitor (s) reaches its conduction level. When the unijunction conducts, a positive transition is coupled across capacitor C38 to the input of NOR gate MC41A (A) driving the output to its low state.

The low state output is capacitively coupled to the input of inverter MC41B producing a position going pulse at its output. This pulse clears the flip-flop comprised of MC77A

and MC77B. The clearing of the flip-flop enables NOR gate MC41C. The next negative transition of the $\overline{800\ \mu s}$ pulse from the time base will set the flip-flop, coupling a positive going pulse across capacitor C24. The positive pulse is inverted by MC77C resulting in a low state output. The low state output from MC77C is coupled across capacitor C26 producing a positive pulse at the output of MC78A. This pulse forward biases transistor Q16 generating the positive going reset pulse. The RC time constant determined by resistor R72 and capacitor C36 fixes the reset pulse duration at approximately 40 μs.

Capacitor C28 couples a negative pulse to the input of inverter MC78B when inverter MC78A returns to its normal low state. The positive going pulse at the output of MC78B, typically 40 μs in duration, forward biases transistor Q17 causing the emitter to go positive generating the preset pulse.

During operation in either of the sampling bands, the parity gate at MC78C will be enabled by the time base circuit. The generation of an error reset signal by the parity circuitry will produce a high level output at MC78C. A positive pulse will be coupled across C29 to 3-input NOR gate, MC77C, generating the reset pulse previously described. However, before inverter MC78A returns to its low state generating the preset pulse, the high state output from MC78C will trigger the storage-transfer one-shot through capacitor C32 and transistor Q21. The RC time delay R84 and C32 permits the storage-transfer pulse to occur after reset resulting in a readout display of all zeros whenever parity detects an error.

3.5.12 120 MHz DCU (C-11-06051)

The 120 MHz DCU (decimal counting unit) is, in essence, the least significant digit of the count chain. As it must be capable of counting frequencies to 120 MHz, the divide-by-ten function is accomplished by a series of MECL high speed logic J-K flip-flop.

The 120 MHz DCU circuitry includes a high gain amplifier, the count gate, a decade of high speed MECL logic and bandswitching logic to enable either the direct input (low band) or the countdown input (mid and high bands).

During low band operation, the direct input signal from the input power divider is coupled to the base of transistor Q201 through capacitor C218. The voltage divider comprised of R201 and R202 maintains the proper bias level on Q201.

Transistors Q201, Q202, Q203 and Q204 amplify the input signal. The bypass capacitors associated with the emitter of each transistor counteract a tendency to oscillate due to the high gain of the stage. The high amplitude signal at the collector of Q204 is limited to approximately 1.5 volts by diodes CR203-CR206. Transistors Q205 and Q206 feed a portion of the output energy back to the emitter of Q201, decreasing the overall gain of the stage. Capacitors C206, C207 and C208 filter the signal to a dc level which, coupled through diodes CR201 and CR202, decreases the dc bias of Q201.

Transistors Q207 and Q208 form a Schmitt trigger, squaring the signal and providing the required MECL logic levels. The output, at the collector of Q208, is coupled directly to the input of MC201A. In low band, the CH. A Enable line will be at a high state while the Test-Override line will be in its low state. The high state (CH. A Enable) is inverted by MC203D and coupled to NOR gate MC203A. The low level Test-Override line is coupled directly to the remaining input of MC203A producing a high level output. The junction of voltage divider R223, R224 will therefore be positive, back biasing Q210, enabling the -5.2 volt supply through R222 to the input of MC201A. Since three of the inputs of MC201A will be at a low level, the direct input from the Schmitt trigger will be enabled to MC202D, the count gate.

With the Test-Override line in its low state, transistor Q212 will be forward biased by voltage divider R234, R235, grounding (high state) one of the inputs of MC202B. This disables the 1 MHz test signal and results in a low state output to MC202D, the count gate. The high state CH. A Enable line will be inverted by MC203C, forward biasing transistor Q213. The collector of Q213 will assume a high (ground) state disabling the countdown input at MC202A. The resulting low state output from MC202A is also coupled to MC202D. The count gate is enabled when the start-stop flip-flop reverse biases transistor Q13 on the reset and control circuitry, opening the count gate lead to the 120 MHz DCU. The voltage divider of R256, R257 produces a low state input to MC202D, enabling the direct input signal from MC201A to MC204, the first of four high speed MECL J-K flip-flops.

During mid or high band operation, the CH. A Enable line from the reset and control circuit will be held in its low state. The high state output from inverter MC203D results in a low state output from MC203A, forward biasing transistor Q210 through voltage divider R223, R224. The collector of Q210 will be at ground (high state) disabling the direct input at MC201A. Since both inputs to MC203C are in their low state, the output will assume a high level. The junction of voltage divider R232, R233 will therefore be positive in respect to ground, reverse biasing transistor Q213. With Q213 held off, the collector

will be at -5.2 volts through R229, enabling the countdown frequency at MC202A. Three of the inputs to the count gate (MC202D) will be in their low state thereby enabling the countdown frequency from MC202A.

The four MECL J-K flip-flops (MC204, 205, 206 and 207) are arranged to provide a 1-2-4-8 BCD output and a divided-by-ten function. The BCD outputs and the divide-by-ten output are buffered by MC208 and MC209 respectively for RTL logic compatibility prior to being coupled to the count chain.

3.5.13 Count Chain (D-11-06053)

The count chain includes the remainder of the DCU's (Decimal Counting Units) and the nine numerical indicator tubes. Each DCU includes a decade counter, storage register and decimal decoder circuit. The decade counters each provide a 1-2-4-8 BCD count to their respective storage registers and a divided-by-ten "carry" to the succeeding decade. The decades count either the direct or countdown input from the 120 MHz DCU for the duration that the count gate is enabled. The Storage-transfer pulse, generated at the conclusion of the measurement internal, transfers the accumulated count in the storage registers to the decimal decoders, which, in turn, enable the appropriate digit within the individual numerical indicator tubes.

The storage register and decimal decoder circuits (MC1 and MC2) for the buffered 120 MHz BCD output are located within the count chain circuitry. The 10^1 decade is driven by the 120 MHz DCU carry output and employs four TTL flip-flops (MC5 and MC6) arranged as a decade counter. The remainder of the DCU's employ conventional CμL 9958 decades.

3.5.14 Power Supply (C-11-06047)

All working voltages required by the instrument are derived from an ac primary power source. Each individual supply is regulated against source variations with the exception of the +230 volt dc unregulated plate supply.

Power to the primary circuit of the power transformer is controlled by front panel POWER switch S301 and protected by fuse F301 (1Amp. MDL for 115 volt operation). The power transformer has two separate 115 volt primary windings. The windings are either placed in series (230 volt operation) or parallel (115 volt operation) by rear panel 115/230 volt line switch S302.

The rear panel mounted fan is designed to operate ONLY from 115 volts and is connected across one of the primary windings. During 230 volt operation, the two primary windings act as an autotransformer, providing the required 115 volts to the fan.

The power transformer incorporates three separate secondary windings to derive the various dc power levels. The unregulated +230 volt dc indicator tube plate supply is referenced to the single secondary. Capacitor C301 filters the rectified high voltage signal from CR301 to the required +230 volt dc level. The remaining dc supplies with the exception of the ±8.2V supply, are referenced to the regulated +12 volt supply.

CR2-5, C302, and C303 provide coarsely filtered levels of ±17.5V to the ±12V regulators. The voltage divider R307-309 established a voltage level, which is compared to the level established by zener diode CR310. CR310 and the error amplifier Q304 are mounted close together physically. Any drift of the zener voltage with temperature will be partly cancelled out by an equal and opposite drift of the B-E drop of the transistor. The output of the error amplifier is fed to the series regulator Darlington pair Q301/Q302. Note that the positive supply for the regulator circuits is drawn from the +230V display supply. The output current of the supply is limited by Q303. If the drop across current sensing resistor R306 is sufficient to turn on Q303, Q303 robs drive current from Q301 and decreases the output voltage. The current limit is about 650 mA. The output voltage is adjustable from about +11 to +13 volts by R308.

Divider R310/CR311/CR312/R311 produces a voltage proportional to the regulated +12V supply and the -12V level. This signal is amplified by error amplifier Q305 and fed to the series regulator Darlington Q306/Q307 to regulate the -12V level. This supply "tracks" with the +12V supply. If the +12V increases by some amount, the -12V level will decrease (go more negative) by the same amount. Diodes CR11 and CR12 compensate for the thermal drift of Q305. Q308 and R316 limit the current output of the supply to about 400 mA.

CR306-308, C304, and C305 provide coarsely filtered levels of about ±8.2V for the low voltage regulated supplies.

Q309 is the error amplifier for the +4.4V supply. It drives the series regulator Darlington Q311/Q312. Q310 and R322 limit the output current to about 3.5 A.

Divider R323/R324 provide the reference level for the -5.2V supply. Q313 is the error amplifier and Q315 the series regulator. Q314 and R328 limit the current to about 400 mA. CR314 provides temperature compensation for Q313.

The voltage drop of CR315 derives a +3.6V level from the +4.4V supply.

3.6 SPECIALIZED COMPONENTS

The UHF circuits of the Model 970 employ two types of specialized semiconductors. In the countdown circuit, two TUNNEL DIODES serve as multivibrators. In the sampler, the sampling pulse is shaped by a STEP RECOVERY DIODE. The latter device is also referred to as a "Snap" diode, a "Pulse shaping" diode, or a "Boff" diode, after its inventor.

3.6.1 Tunnel Diodes

The tunnel diode is a bistable semiconductor device developed in Japan in the late 1950's. It is occasionally called an Esaki diode, after its inventor. The device is always used in its forward conduction mode. A typical I-V curve for the device is shown below.

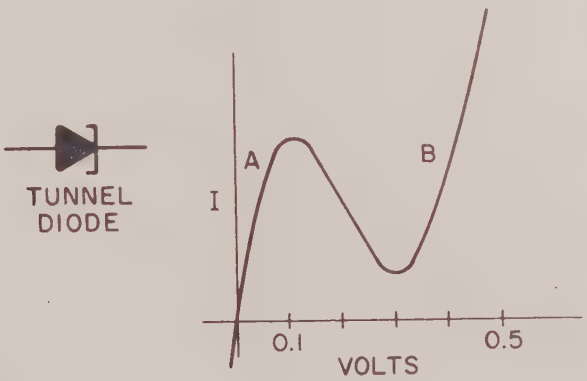


FIGURE 3-14

TUNNEL DIODE

Note that there are two positive-slope regions on the curve, labeled A and B. When the diode is in state A it is considered "off", and when it is in state B it is considered "on". As long as the current through the diode stays below a certain critical level, I_1, the diode will remain in state A. The drop across the diode is typically 100 mV. When the

current exceeds I_1, the diode will switch very rapidly to its high-voltage state. Its voltage drop increases to approximately 0.5V. The state transition takes place in a few picoseconds. The diode will stay on until its current drops below a second level, I_2 (I_2 is typically one quarter of I_1.

The tunnel diodes in the Model 970 are used as oscillators. Each is connected through an inductor to a high-impedance, low-voltage power source.

When the voltage at the tunnel diode is low, the current thru the diode exceeds I_1 (in this case about 10 mA) and the diode turns on. The increased voltage at the diode decreases the current below I_2 and the diode returns to its original state. The steps repeat and the circuit oscillates. The period of the oscillation is determined by the current through the diode and the value of the inductance.

3.6.2 Step Recovery Diodes

The step recovery diode is a highly specialized silicon device used principally in UHF frequency multipliers and high-speed pulse shapers. When a step recovery diode is switched from its conducting to its non-conducting state, it releases its stored charge in one very fast pulse.

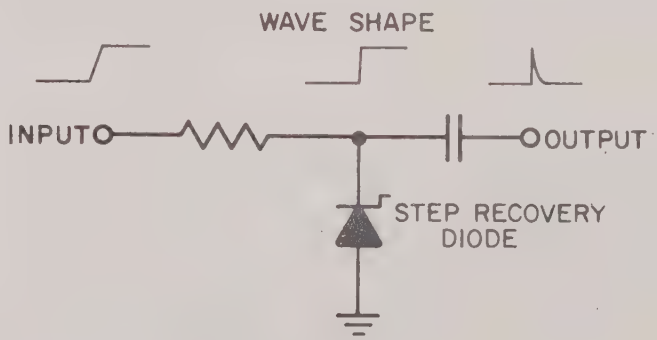


FIGURE 3-15

STEP RECOVERY DIODE

If the diode is connected in the configuration above, it will effectively speed the risetime of a pulse. This configuration is used in the Model 970 sampler circuit to form the very fast sampling pulse.

SECTION 4

MAINTENANCE - CALIBRATION

SECTION 4

MAINTENANCE - CALIBRATION

4.1 INTRODUCTION

Section 4 presents pertinent information to aid in maintaining the factory-new performance of the 970 Frequency Counter. Routine maintenance and calibration procedures are includes with part location drawings, schematic diagrams and integrated circuit equivalents complementing the various procedures. Table 4-1 offers a list of suggested test equipment required for instrument calibration (equivalent equipment acceptable).

TABLE 4-1

RECOMMENDED TEST EQUIPMENT

INSTRUMENT DESCRIPTION	MANUFACTURER AND MODEL	MINIMUM REQUIREMENTS
Digital Volt Meter	Eldorado Model 1820	0.01% accuracy
Oscilloscope	Tektronix Series 580	80 MHz bandwidth
LF Signal Generator	HP202C	Combined range from 20 Hz to 3 GHz
HF Signal Generator	HP606A	
VHF Signal Generator	HP608C	
UHF Signal Generator	HP612A	
UHF Signal Generator	HP614A	
UHF Signal Generator	HP616B	
Frequency Standard	Any	10 times internal oscillator accuracy.

4.2 PERIODIC MAINTENANCE

Periodic maintenance for the 970 Frequency Counter is limited to only routine cleaning of the instrument and air filter. Under normal operating conditions, 90 day maintenance intervals are suggested. Table 4-2 outlines the periodic maintenance procedure.

TABLE 4-2

PERIODIC MAINTENANCE

STEP	ACTION
1	Place the POWER switch to the OFF position and disconnect the line cord from the source.
2	Remove the two phillips head screws securing the filter bracket to the rear panel.
3	Cleanse the mesh filter element in a mild household detergent solution, rinse thoroughly and dry. Spray the filter element with a commercial type filter coating (RP filter coat or equivalent).
4	Remove the top and bottom cover panels by extracting the 5 #4 phillips head screws securing each panel to the chassis and sliding the panels back towards the rear of the instrument.
5	Clean the interior of the instrument if necessary, with CLEAN, DRY compressed air. Prior to replacing the cover panels, check the physical integrity of the plug-in P.C. boards and coaxial connectors.
6	Replace the filter element and bracket. The exterior of the instrument may be cleaned with an equal part solution of denatured alcohol and water - stronger solvents may damage the finish or polaroid lens.

4.3 CALIBRATION

Periodic adjustment of the internal oscillator is the only normal calibration requirement for the 970. The remaining internal adjustments, originally set at the factory, are not subject to periodic calibration.

The output frequency of the oscillator may be adjusted relative to a 1 MHz frequency standard by observing the rotation rate of a Lissajous pattern as depicted by the test configuration in Figure 4-1. For optimum counter operation, the oscillator should be

calibrated after 30 days of operation and at 90 day intervals thereafter. As oscillator aging is greatest when it is first placed in operation, instrument power should be maintained whenever possible. Table 4-3 outlines the calibration procedure for the internal oscillator.

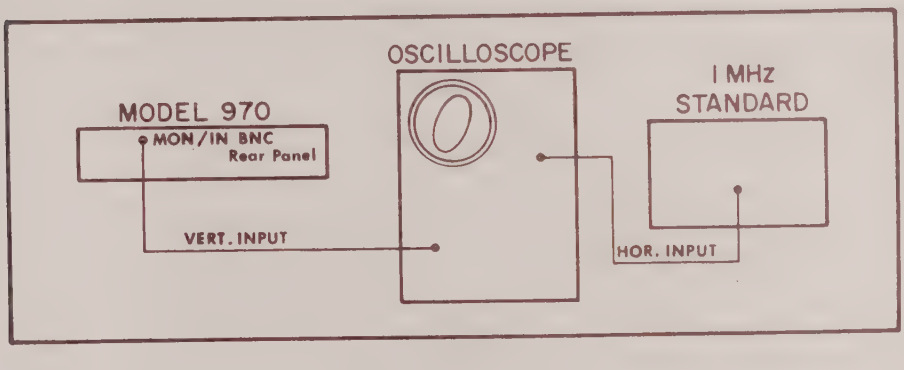


FIGURE 4-1

OSCILLATOR TEST CONFIGURATION

TABLE 4-3

OSCILLATOR CALIBRATION

STEP	ACTION
1	Apply instrument power and allow a minimum of 30 minutes continuous operation for oscillator stabilization.
2	Connect the oscilloscope's vertical input to the rear panel MON/IN BNC connector and place the INT-EXT switch to the INTernal position.
3	Connect the 1 MHz frequency standard to the oscilloscope's horizontal input and set the horizontal input switch to external.
4	Adjust the oscilloscope for a Lissajous pattern of convenient amplitude.

TABLE 4-3 (Continued)

STEP	ACTION
5	Remove the top cover panel by extracting the 5 #4 phillips head screws securing the cover to the chassis.
6	While observing the oscilloscope, adjust variable capacitor C1 on the logic P.C. board for minimum rotation (refer to Figure 4-2).
7	Replace the top cover panel and secure it in place with two or three screws.
8	Observe the pattern for five minutes noting Lissajous rotation rate. If the rotation rate increases, remove the top cover panel and readjust capacitor C1 for minimum rotation. Again replace the cover panel and observe the rotation rate for five minutes. Continue to monitor and adjust the oscillator until minimum rotation is realized. The cover panel must be in place as it affects both capacitance and internal temperature.
9	Disconnect the cable from the MON IN BNC connector and replace the cover panel using all 5 screws. Note the date for the next required calibration.

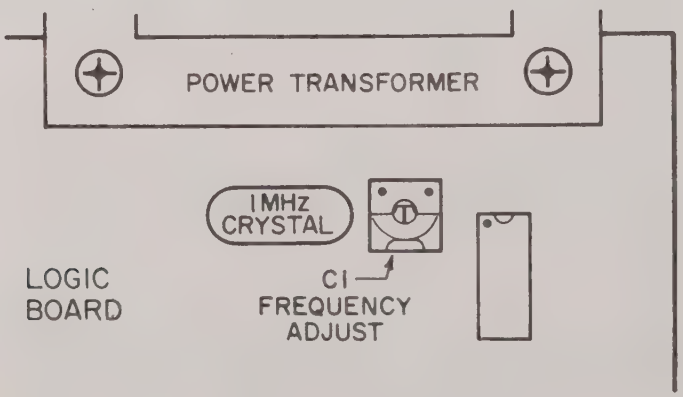


FIGURE 4-2

OSCILLATOR COMPONENT LOCATION

4.4 INTERNAL ADJUSTMENTS

With the exception of the oscillator, the internal calibration adjustments require no periodic compensation. Calibration of these "semi-fixed" adjustments is necessitated only if a component is replaced or if a decrease in performance specifications is apparent.

4.4.1 Power Supply Adjustment

The +12 volt dc supply is the reference for the -12V and -5.2V regulated supplies and incorporates the only power supply adjustment. Table 4-4 outlines the power supply calibration procedure.

NOTE

> Readjustment of the power supply requires complete calibration of the instrument including the internal oscillator and all semi-fixed adjustments.

TABLE 4-4

POWER SUPPLY CALIBRATION

STEP	ACTION
1	Remove the top cover panel by extracting the five phillips head screws securing the cover in place and sliding the cover towards the rear of the instrument.
2	Connect one lead of the DVM to chassis ground and the other lead to the +12V bus wire from the mother board to the 120 MHz DCU P.C. Board (front-left corner of the 120 MHz DCU).
3	Adjust potentiometer R308 on the logic board (Figure 4-3) for +12 volts ±100 mV.
4	Monitor the adjacent -12V bus wire for -12 volts ±100 mV. It may be necessary to slightly readjust the +12 volt supply to bring both supplies within ±100 mV.

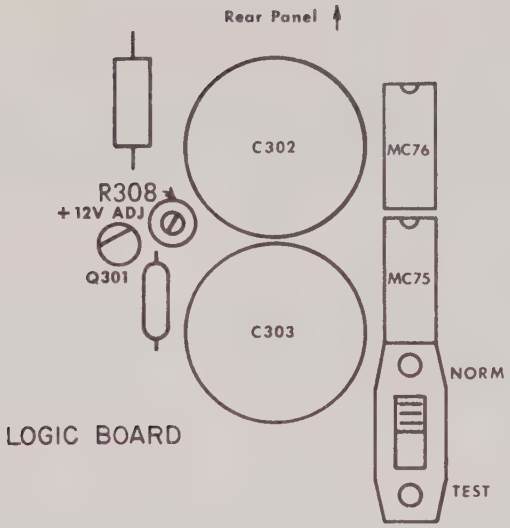


FIGURE 4-3

POWER SUPPLY ADJUSTMENT LOCATION

4.4.2 Countdown Bias Adjustment

The bias current to the mid and high band tunnel diode multivibrators determines their overall range of operation. Variable resistors R15 and R31 are set for ranges of 8.75 to 9.75 MHz (mid band) and 32-36 MHz (high band) respectively. Table 4-5 outlines the procedure for adjusting the countdown bias current. The only test equipment required is a +4 volt dc source, either a filtered laboratory supply or a voltage divider from the instrument's +12 volt supply.

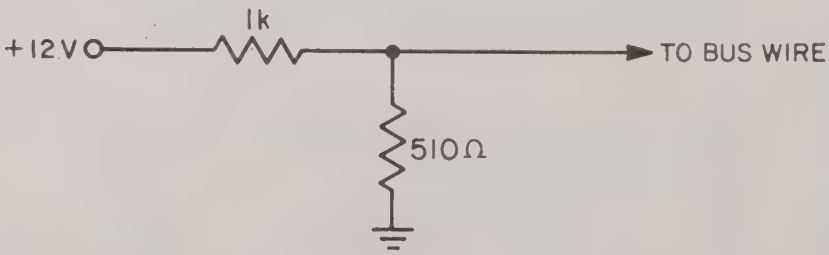


FIGURE 4-4

+4 VOLT VOLTAGE DIVIDER

TABLE 4-5

COUNTDOWN BIAS ADJUSTMENT

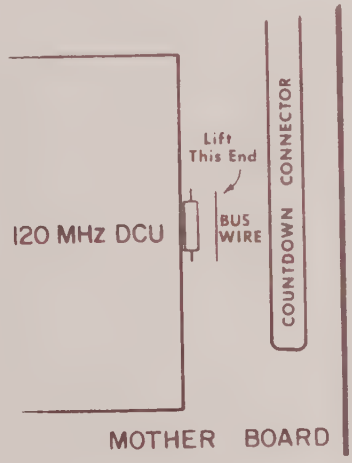
STEP	ACTION
1	Disconnect instrument power and remove the top cover panel.
2	With a pneumatic solder extractor, remove the rear lead of the teflon-covered bus wire located on the right side of the mother board between the 120 MHz DCU and the countdown circuit's PC board connector.  It may be necessary to first remove the countdown PC board to gain ample access to the bus wire.
3	Apply instrument power and place the TEST/NORMAL switch, in the TEST position (refer to Figure 4-3). This enables the display to read the countdown output frequency directly (disregard the decimal point location).
4	Ground the free end of the bus wire previously removed in Step 2.
5	Rotate the MODE/RANGE switch to the 110-700 MHz (mid-band) position. Do NOT apply an input signal.
6	The display should indicate 8.75 MHz or less. If it does not, adjust potentiometer R15 accordingly (refer to Figure 4-5).

TABLE 4-5 (Continued)

STEP	ACTION
7	Remove the ground from the bus wire and apply a +4 volt dc level.
8	The display should exceed 9.75 MHz. Readjust potentiometer R15 as necessary to provide an overall range of 8.75 to 9.75 MHz.
9	Place the MODE/RANGE switch to the 0.6 - 3.2 GHz (high-band) position.
10	The display should now indicate 36 MHz or greater. If not, adjust potentiometer R31 until a reading of at least 36 MHz is realized.
11	Remove the +4 volt dc level and ground the bus wire.
12	The display should indicate 32 MHz or less. Readjust potentiometer R31 as necessary to provide an overall range of 32 to 36 MHz.
13	Return the TEST/NORM switch to the NORM position and resolder the bus wire in place if no further internal adjustments are required.

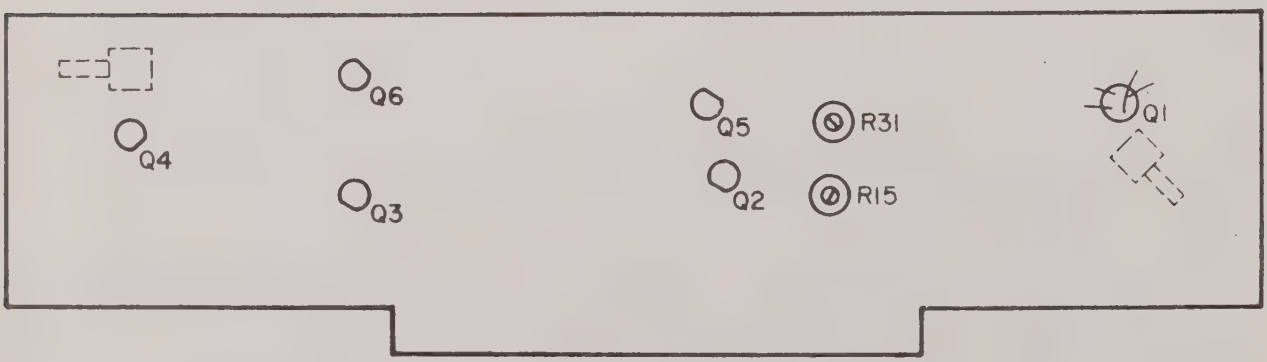


FIGURE 4-5

COUNTDOWN ADJUSTMENT LOCATION

4.4.3 Frequency Synthesizer Balance Adjustment

The 90° phase shifter networks for the frequency synthesizer's balanced modulators incorporate two trimmer capacitors to attain the required fine phase separation. Table 4-6 outlines this adjustment procedure.

TABLE 4-6

FREQUENCY SYNTHESIZER BALANCE ADJUSTMENT

STEP	ACTION
1	Apply a +4 volt dc level to the free end of the bus wire (refer to Table 4-5, step 2).
2	Externally trigger the oscilloscope with the 5 kHz (Δf) square wave at TP1 (top of R134) on the mother board (refer to Figure 5-3). Set the oscilloscope time base to 50 μs/cm and amplitude to 0.05V/cm.
3	Rotate the MODE/RANGE switch to the 0.6 - 3.2 GHz position (high-band). Do NOT apply an input signal.
4	Connect the oscilloscope's vertical input to the base of transistor Q11 (refer to Figure 4-6). Use a times-ten probe.
5	The signal displayed will be a high frequency sinewave with some degree of modulation with the 5 kHz Δf signal.
6	Alternately adjust variable capacitor C17 and variable resistor R43 for minimum modulation. Figures 4-7A and 4-7B depict improper and ideal waveforms respectively. Use a non-metallic alignment tool taking care to remove both tool and hand from the immediate vicinity of the adjustments when observing the output waveform.
7	Place the MODE/RANGE switch to mid band (110-700 MHz). Remove the probe from the base of transistor Q11 and connect it to the base of transistor Q6.

TABLE 4-6 (Continued)

STEP	ACTION
8	Adjust variable capacitor C2 for minimum modulation as described in step 6. Do not readjust the setting of variable resistor R43.
9	Disconnect instrument power and remove the +4 volt dc level. Replace the bus wire to its normal position and solder it in place.

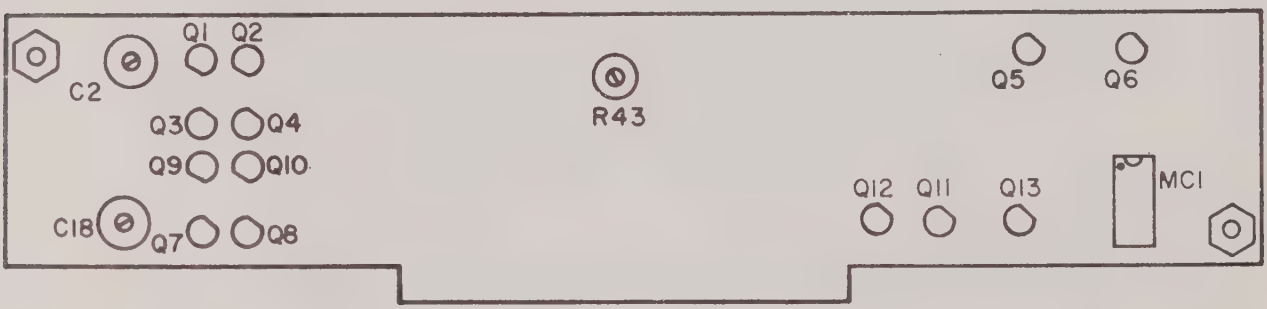


FIGURE 4-6

FREQUENCY SYNTHESIZER ADJUSTMENT LOCATION

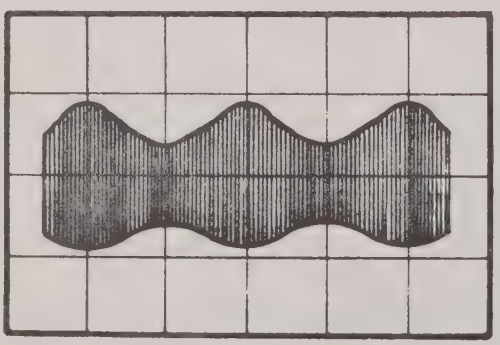


FIGURE 4-7A

IMPROPER WAVEFORM

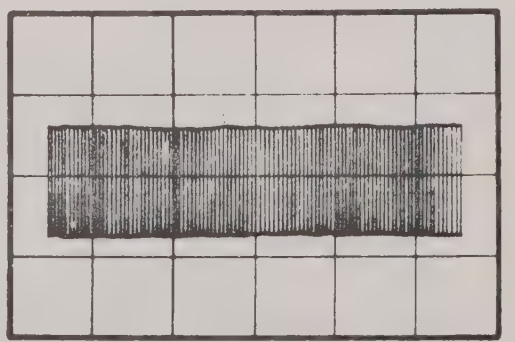


FIGURE 4-7B

IDEAL WAVEFORM

4.4.4 Sampler Bias Adjustment

The sampler bias adjustment determines the shape of the sampling pulse. This pulse, however, is not observable directly. The procedure outlined in Table 4-7 explains how the sampler is adjusted for best performance.

TABLE 4-7

INPUT SAMPLER BIAS ADJUSTMENT

STEP	ACTION
1	Place the POWER switch to the ON position and select the high band (0.6 - 3.2 GHz).
2	Apply an input signal of approximately 3 GHz to the Input connector.
3	Set the input amplitude to provide a consistant reading.
4	Gradually decrease the input amplitude. Adjust variable resistor R49 for maximum sensitivity (refer to Figure 4-8).
5	Continue to decrease the input amplitude while adjusting R49 until maximum sensitivity is realized.
6	This completes the internal adjustments, place the POWER switch to the OFF position and replace the top cover panel using all five phillips head screws.

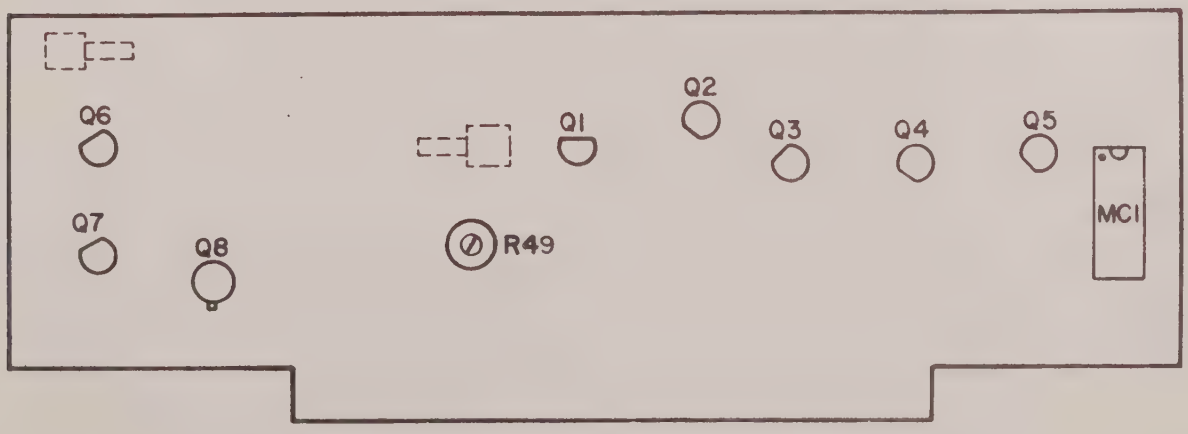


FIGURE 4-8

SAMPLER BIAS ADJUSTMENT LOCATION

4.5 REPAIR

In the event of a suspected failure and before any troubleshooting or repairs are attempted:

1. Read the WARRANTY enclosed at the front of this manual.

2. Insure that the applied input is of sufficient amplitude and within the specified frequency range.

3. Verify proper positioning of all operating controls.

If a valid malfunction is encountered, first insure that all dc power levels are present and correct before attempting to sectionalize the malfunction. Section 3, the theory of operation, will prove a valuable aid in fault location.

4.6 REPAIR TECHNIQUES

Repair of the instrument whould be undertaken only by qualified personnel adept in solid state repair techniques. When a component failure is encountered, observe these general instructions:

1. Never remove or replace a component or P.C. board while instrument power is enabled.

2. Use only a grounded, transformer-coupled, thermostatically controlled soldering iron.

3. Avoid any application of acid-core type solder.

4.6.1 UHF PC Board Removal

To remove any of the UHF PC boards mounted on the mother board:

1. Remove the top cover panel.

2. Unplug any cables connected to the PC board to be removed. If the cable is permanently fastened to the PC board, cut any cable ties involved to remove the cable from its terminal location.

3. To gain access to the 120 MHz DCU, or the transistors beneath it, unsolder the electrolytic capacitor, the copper ground strap, and the three bus wires along the front edge of the PC board. Remove the four phillips-head screws that hold the DCU in place the fold the card upward, bending the leads along the left edge.

4.6.2 Power Transistor Replacement

In the event that any of the plastic power transistors fail, proceed as follows:

1. Carefully remove each wire lead to the defective transistor.

2. Remove the hardware securing the transistor to its mounting.

3. Coat both sides of the mica insulating washer with a heat conductive grease (Dow Corning compound 107 or equivalent).

4. Align the mica washer with the hole in the transistor mounting plate and install the replacement transistor with the exposed metallic portion towards the mica washer. Secure the transistor in place with the exsiting hardware.

5. Solder the transistor in place and trim the leads as warranted.

4.6.3 Integrated Circuit Replacement

1. Verify that the integrated circuit in question is, in deed, defective (refer to the integrated circuit equivalent diagrams contained in Section 4.7).

2. At the component side of the P.C. board, carefully clip each lead of the defective integrated circuit at the point where the lead enters the plastic case.

3. Carefully remove each individual lead from the component side of the P.C. board with the aid of a soldering iron and long nose pliers.

4. Remove all excess solder with a pneumatic solder extractor.

5. Install the replacement integrated circuit noting correct orientation as depicted by the respective component location illustration.

6. Solder each lead on the circuit side and all top traces on the component side of the P.C. Board.

4.7 INTEGRATED CIRCUIT EQUIVALENTS

Circuit equivalents for each type of integrated circuit are described in numerical sequence within this section. If further information is required, refer to the manufacturer's description.

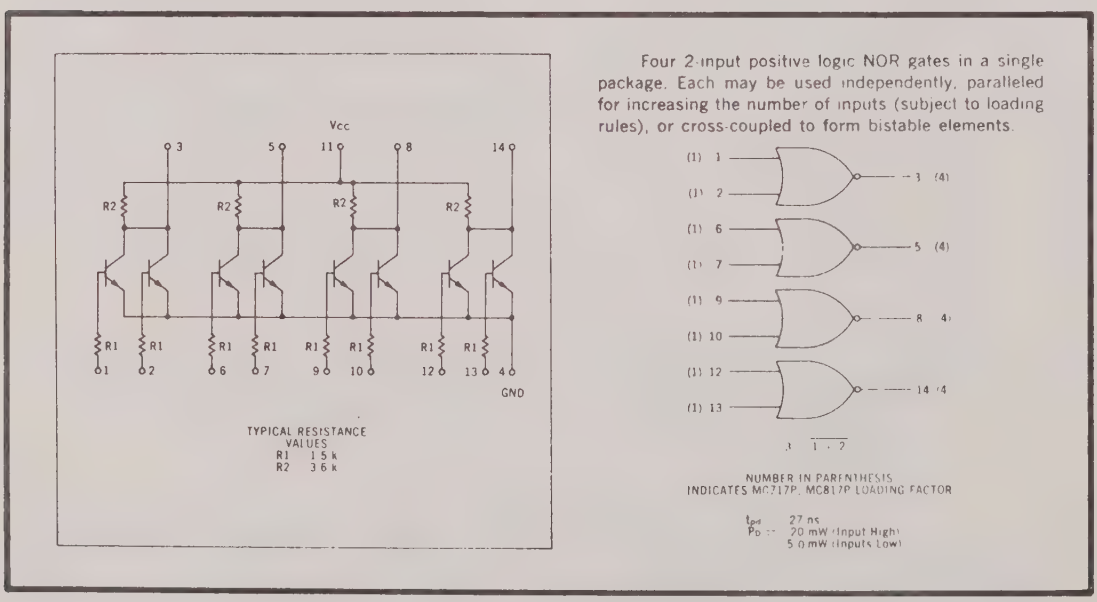


FIGURE 4-9

MC717P EQUIVALENT

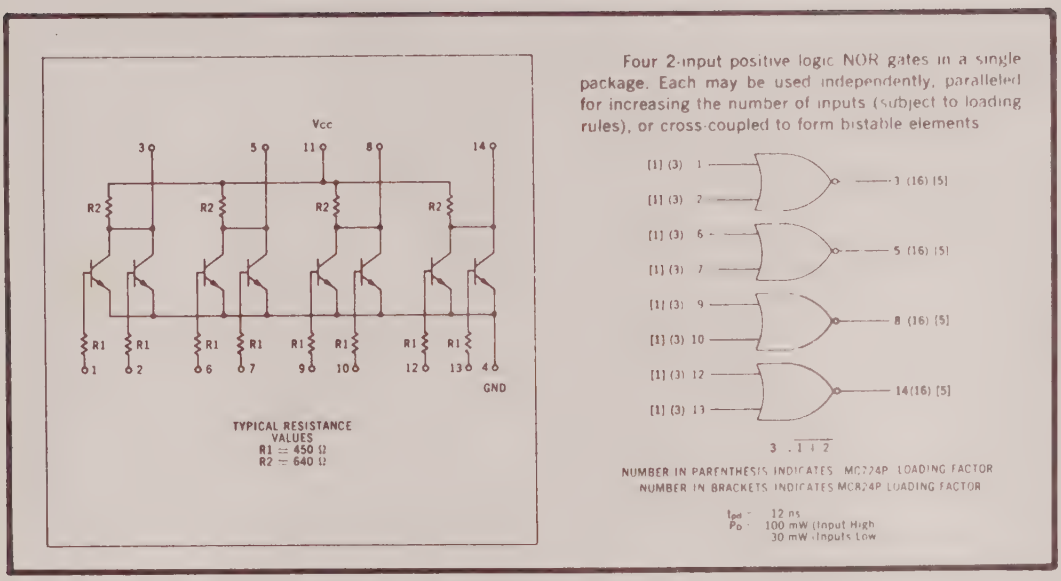


FIGURE 4–10

MC724P EQUIVALENT

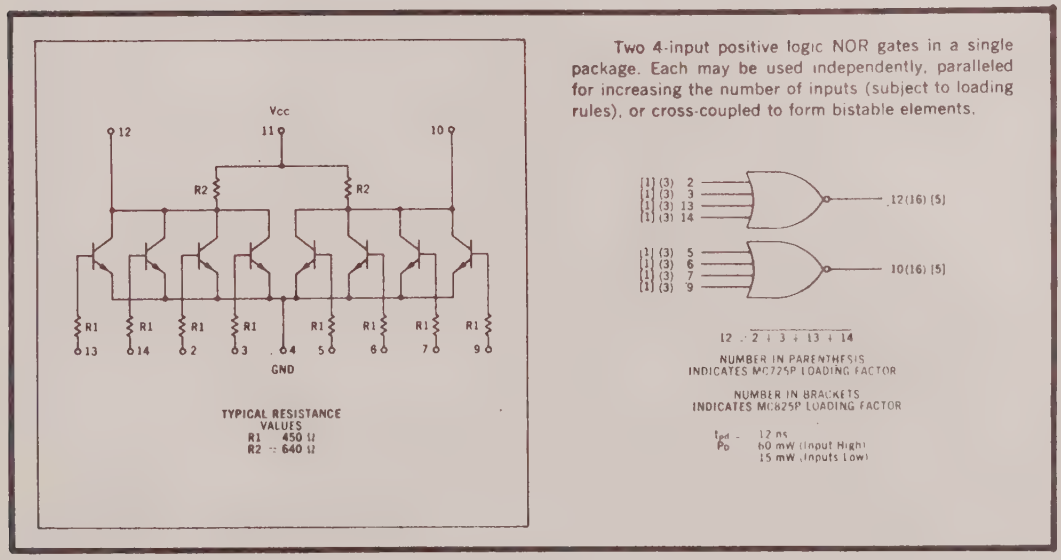
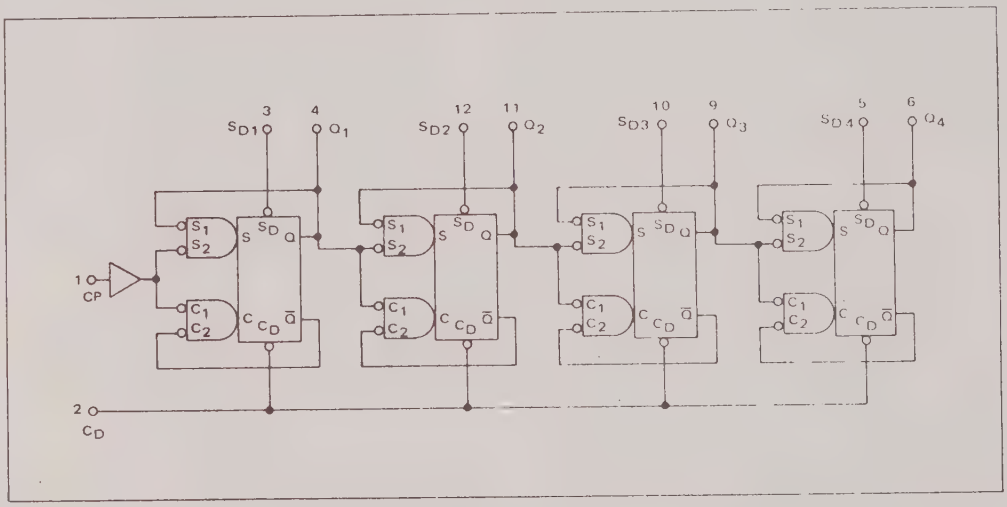


FIGURE 4–11

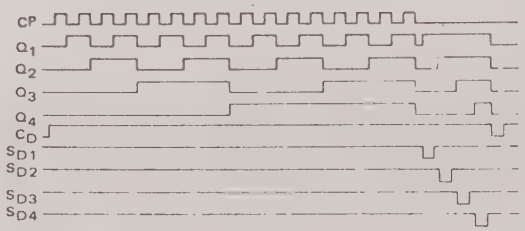
MC725P EQUIVALENT

This monolithic ripple counter is designed to operate at ±20% of the nominal 5.0 volt power supply voltage and is guaranteed to 20 MHz. It has standard MDTL inputs, and uses active pull-up devices in the outputs to increase capacitive drive capabilities. The outputs correspond to a standard 8-4-2-1 binary code with individual direct sets and a common direct clear available to preset the counter to any desired condition. Typical noise margin in 1.0 volt.

Input Loading Factor
S_D = 1.5
C_D = 5
CP = 1
Output Loading Factor = 8
Total Power Dissipation = 150 mW typ/pkg
Maximum Counting Frequency = 30 MHz typ



COUNTER SEQUENCE



DECODING LOGIC

0	$\bar{Q}_1$	$\bar{Q}_2$	$\bar{Q}_3$	$\bar{Q}_4$
1	Q_1	$\bar{Q}_2$	$\bar{Q}_3$	$\bar{Q}_4$
2	$\bar{Q}_1$	Q_2	$\bar{Q}_3$	$\bar{Q}_4$
3	Q_1	Q_2	$\bar{Q}_3$	$\bar{Q}_4$
4	$\bar{Q}_1$	$\bar{Q}_2$	Q_3	$\bar{Q}_4$
5	Q_1	$\bar{Q}_2$	Q_3	$\bar{Q}_4$
6	$\bar{Q}_1$	Q_2	Q_3	$\bar{Q}_4$
7	$\bar{Q}_1$	Q_2	Q_3	$\bar{Q}_4$
8	$\bar{Q}_1$	$\bar{Q}_2$	$\bar{Q}_3$	Q_4
9	Q_1	$\bar{Q}_2$	$\bar{Q}_3$	Q_4
10	$\bar{Q}_1$	Q_2	$\bar{Q}_3$	Q_4
11	Q_1	Q_2	$\bar{Q}_3$	Q_4
12	$\bar{Q}_1$	$\bar{Q}_2$	Q_3	Q_4
13	Q_1	$\bar{Q}_2$	Q_3	Q_4
14	$\bar{Q}_1$	Q_2	Q_3	Q_4
15	Q_1	Q_2	Q_3	Q_4

FIGURE 4-12

MC839P EQUIVALENT

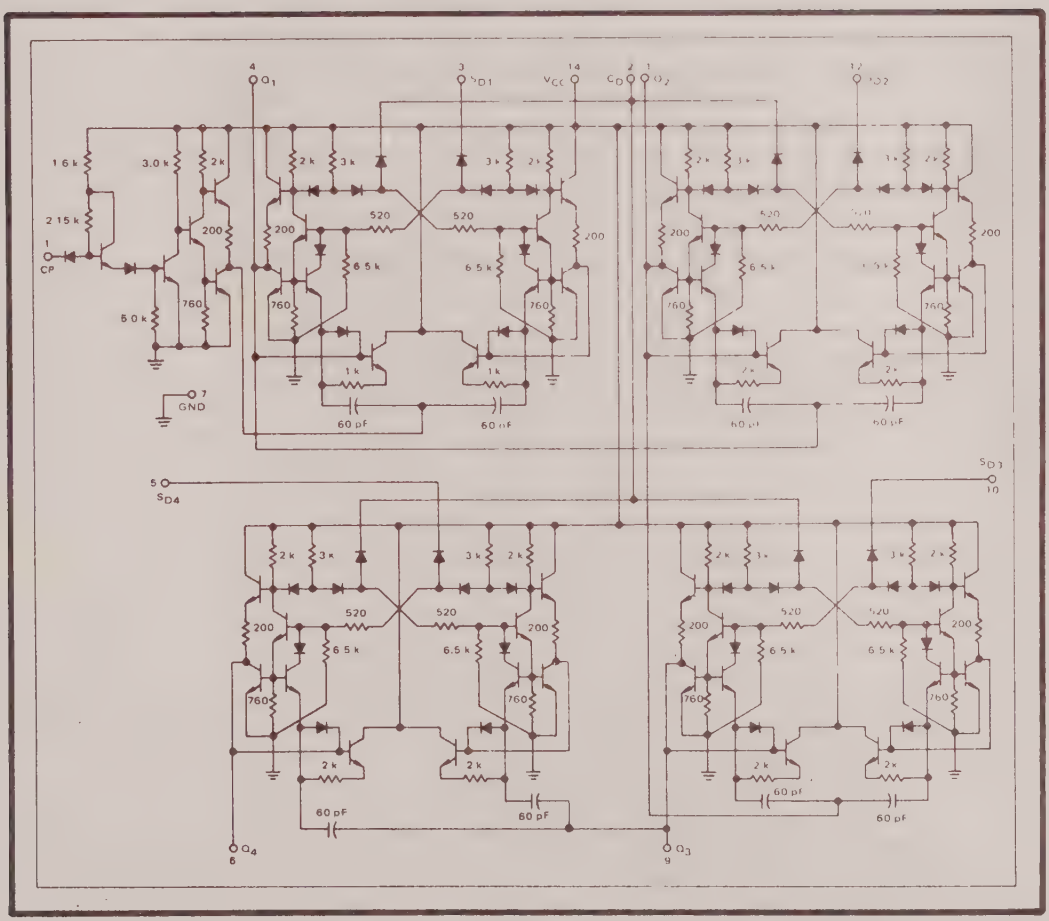
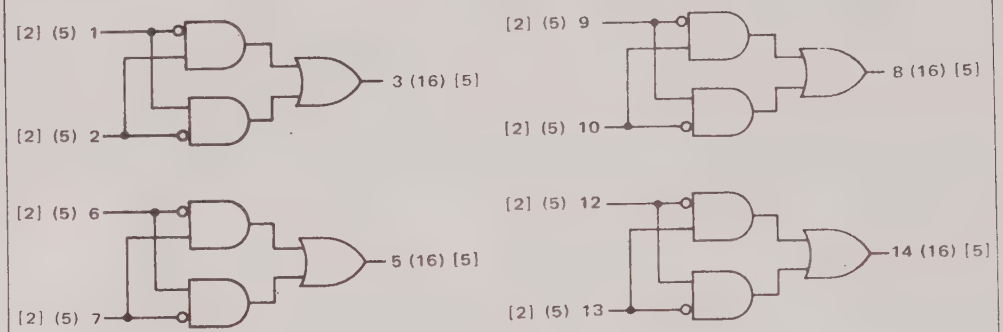


FIGURE 4-13

MC839P SCHEMATIC

Four gate arrays designed to provide the Exclusive OR function. The output is high only if one input is high and all other inputs are low.

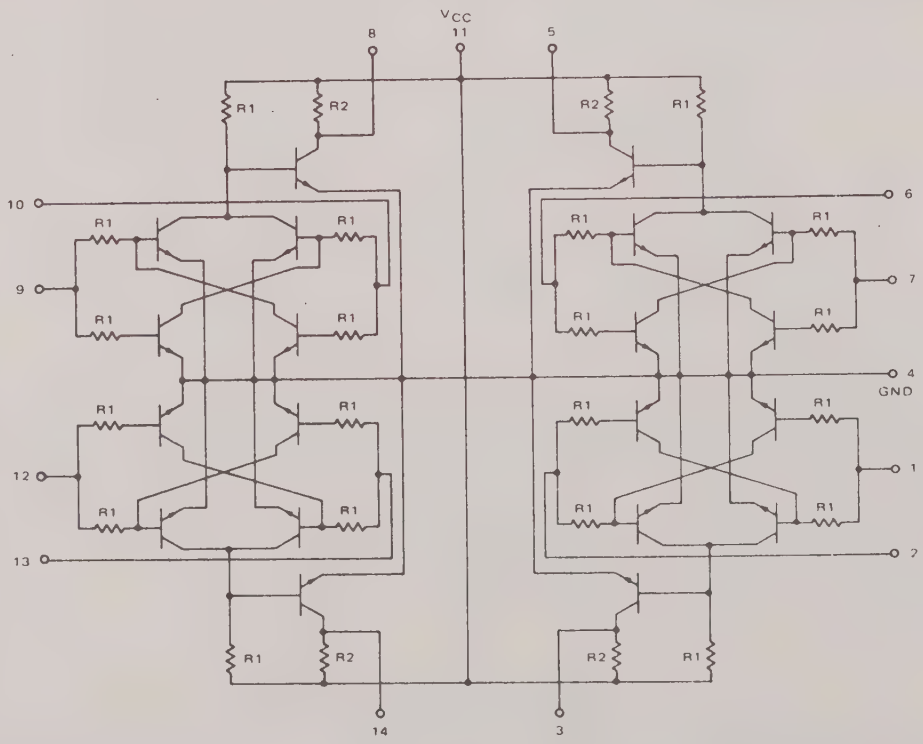


POSITIVE LOGIC
$3 = 1 \cdot \overline{2} + \overline{1} \cdot 2$

t_{pd} = 12 ns typ
P_D = 87 mW typ

NUMBER IN PARENTHESIS INDICATES LOADING FACTOR FOR MC771P

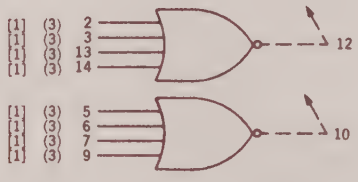
NUMBER IN BRACKETS INDICATES LOADING FACTOR FOR MC871P



Typical Resistance Values
R1 = 450 Ω
R2 = 640 Ω

FIGURE 4-14
MC771P EQUIVALENT

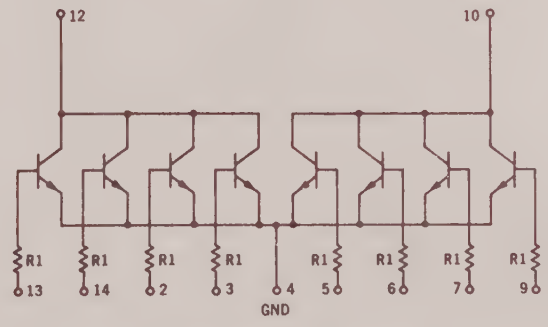
Two 4-input gate expanders housed in a single package. Each may be used independently or combined. Each expander increases the input capability of a standard MRTL gate by four.



$12 = \overline{2 + 3 + 13 + 14}$

$t_{pd} = 12$ ns
$P_D = 20$ mW (Input High)
Negligible (Inputs Low)

NUMBER IN PARENTHESIS INDICATES MC786P LOADING FACTOR.
NUMBER IN BRACKETS INDICATES MC886P LOADING FACTOR.
SEE SHEET 6-158 FOR EXPANDER RULES



V_{CC} CONNECTION TO PIN 11 NOT SHOWN

TYPICAL RESISTANCE VALUES
R1 = 450 Ω

FIGURE 4-15

MC786P EQUIVALENT

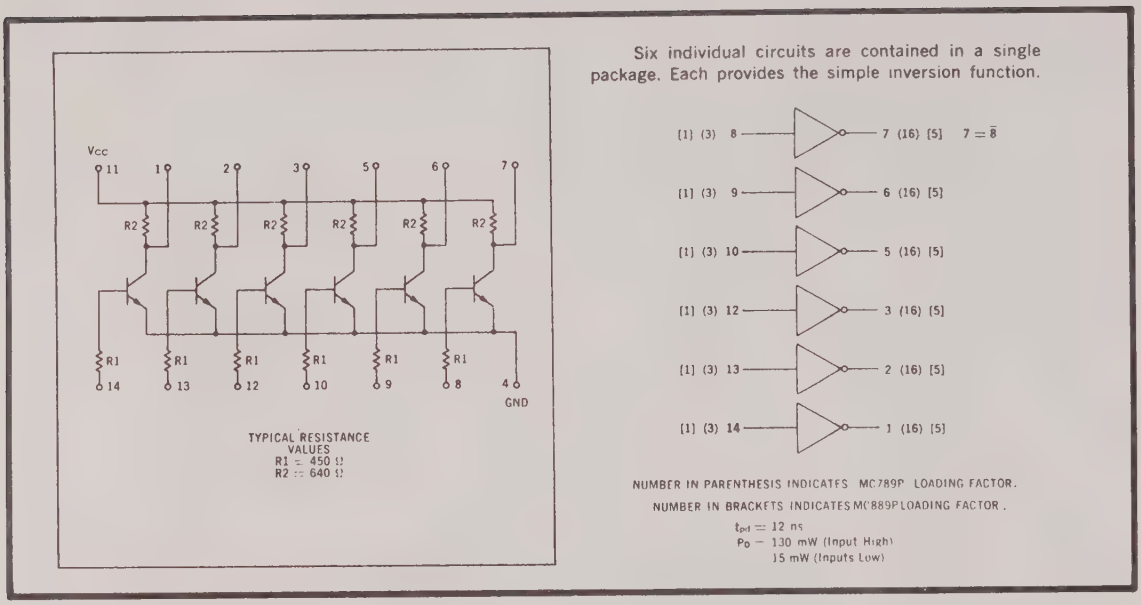


FIGURE 4-16

MC789P EQUIVALENT

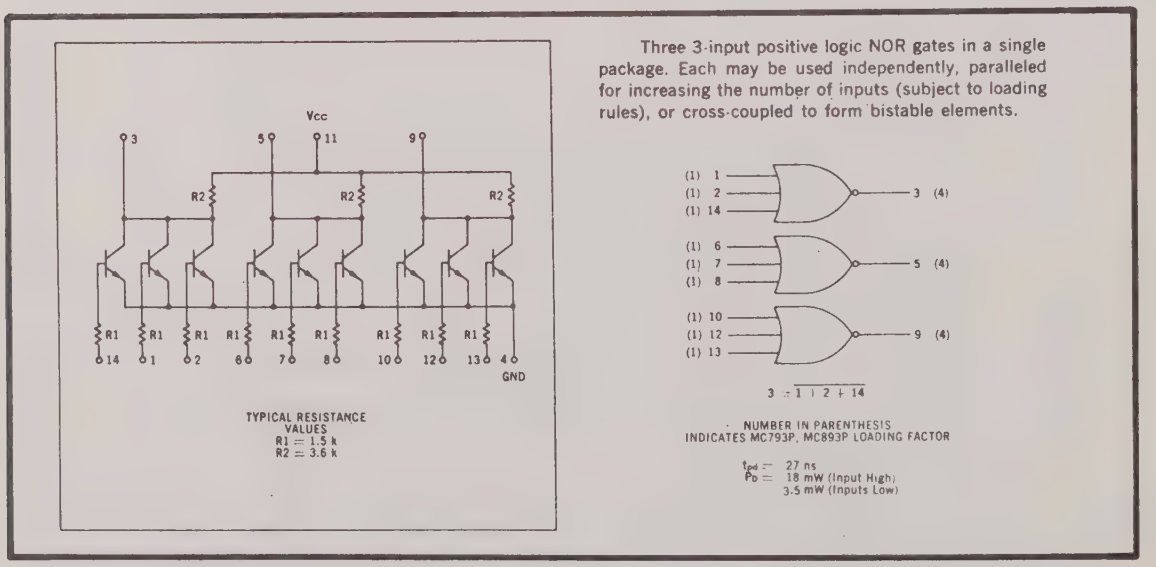
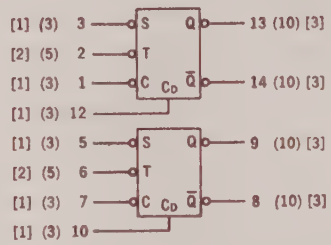


FIGURE 4-17

MC793P EQUIVALENT

Two J-K flip-flops in a single package. Each flip-flop has a direct clear input in addition to the clocked inputs.



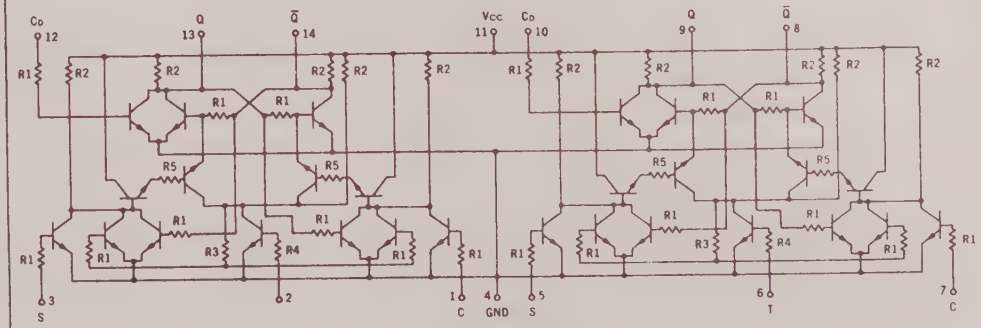
f_{tog} = 4 MHz
P_D = 182 mW (Only Clock Input High)
158 (Inputs Low)

CLOCKED INPUT OPERATION (1)

t_n (2)		t_{n+1} (2)	
S	C	Q	$\bar{Q}$
1	1	Q_n (3)	$\bar{Q}_n$
1	0	1	0
0	1	0	1
0	0	$\bar{Q}_n$	Q_n (3)

1. Direct input (C_D) must be low.
2. The time period prior to the negative transition of the clock pulse is denoted t_n and the time period subsequent to this transition is denoted t_{n+1}.
3. Q_n is the state of the Q output in the time period t_n.
4. Clock pulse fall time must be < 100 ns.

NUMBER IN PARENTHESIS INDICATES LOADING FACTOR FOR MC790P
NUMBER IN BRACKETS INDICATES LOADING FACTOR FOR MC890P

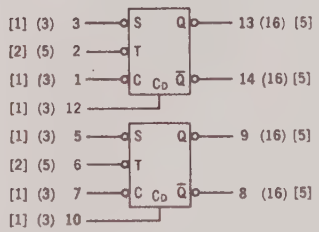


TYPICAL RESISTANCE VALUES
R1 = 450 Ω R3 = 510 Ω
R2 = 640 Ω R4 = 225 Ω
R5 = 300 Ω

FIGURE 4-18

MC790P EQUIVALENT

Two J-K flip-flops in a single package. Each flip-flop has a direct clear input in addition to the clocked inputs.



f_{reg} = 4 MHz
t_{pd} = 40 ns typ

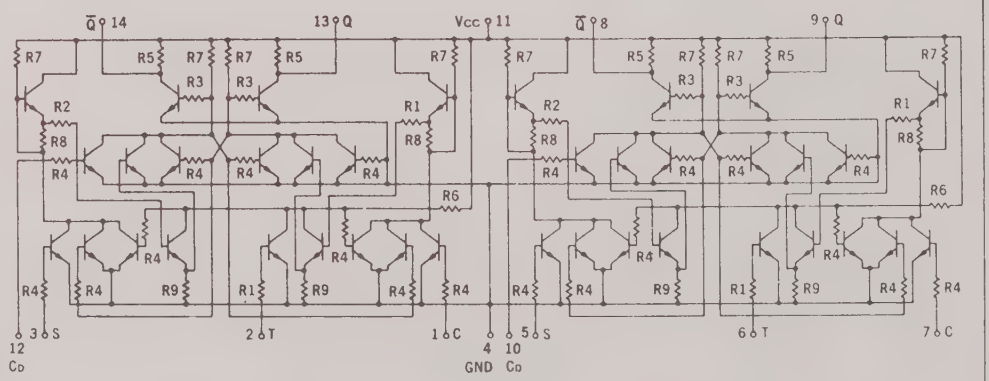
P_D = 190 mW typ (Only Clock Input High)
160 mW typ (Inputs Low)

CLOCKED INPUT OPERATION (1)

t_n (2)		t_{n+1} (2)	
S	C	Q	$\bar{Q}$
1	1	Q_n (3)	$\bar{Q}_n$
1	0	1	0
0	1	0	1
0	0	$\bar{Q}_n$	Q_n (3)

1. Direct input (C_D) must be low.
2. The time period prior to the negative transition of the clock pulse is denoted t_n and the time period subsequent to this transition is denoted t_{n+1}.
3. Q_n is the state of the Q output in the time period t_n.

NUMBER IN PARENTHESIS INDICATES LOADING FACTOR FOR MC791P
NUMBER IN BRACKETS INDICATES LOADING FACTOR FOR MC891P

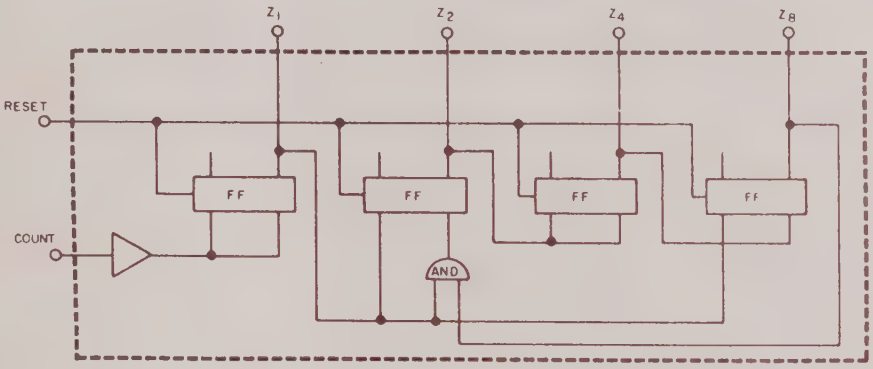


TYPICAL RESISTANCE VALUES

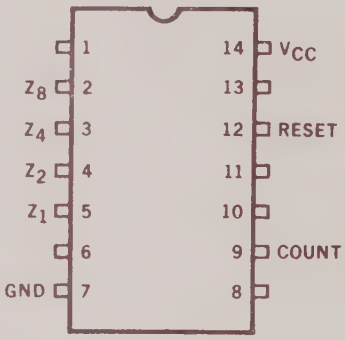
R1	300 Ω	R4	600 Ω	R7	900 Ω
R2	500 Ω	R5	640 Ω	R8	2.0 k
R3	550 Ω	R6	700 Ω	R9	3.0 k

FIGURE 4-19

MC791P EQUIVALENT



BLOCK DIAGRAM



	0	1	2	3	4	5	6	7	8	9
Z_1	H	L	H	L	H	L	H	L	H	L
Z_2	H	H	L	L	H	H	L	L	H	H
Z_4	H	H	H	H	L	L	L	L	H	H
Z_8	H	H	H	H	H	H	H	H	L	L

(H = HIGH L = LOW)

TRUTH TABLE

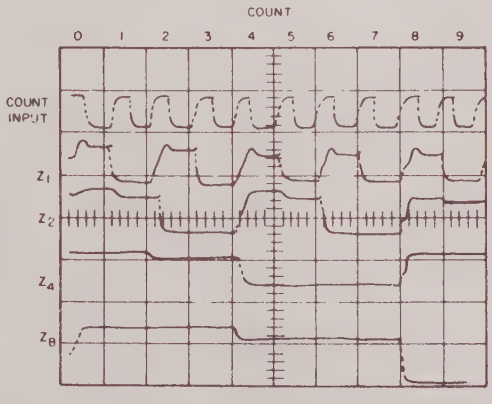
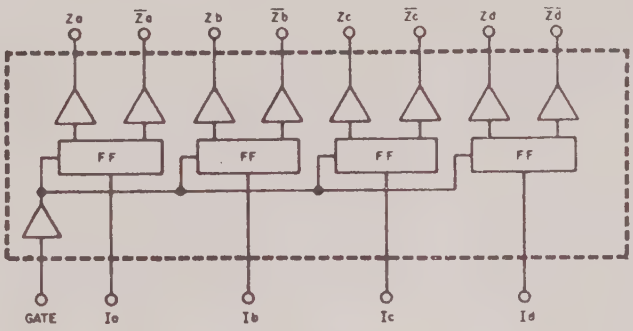
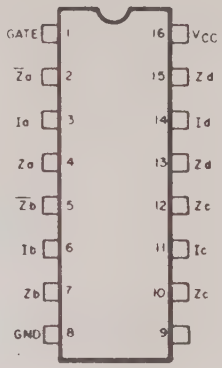


FIGURE 4-20

CμL 9958 EQUIVALENT



BLOCK DIAGRAM



BASE CONNECTIONS

GATE	I	Z	$\overline{Z}$
L	L	L	H
L	H	H	L
H	ANY	Q	$\overline{Q}$

H = HIGH
L = LOW
Q = THE STATE ASSUMED PRIOR TO "GATE HIGH" IS MAINTAINED

TRUTH TABLE

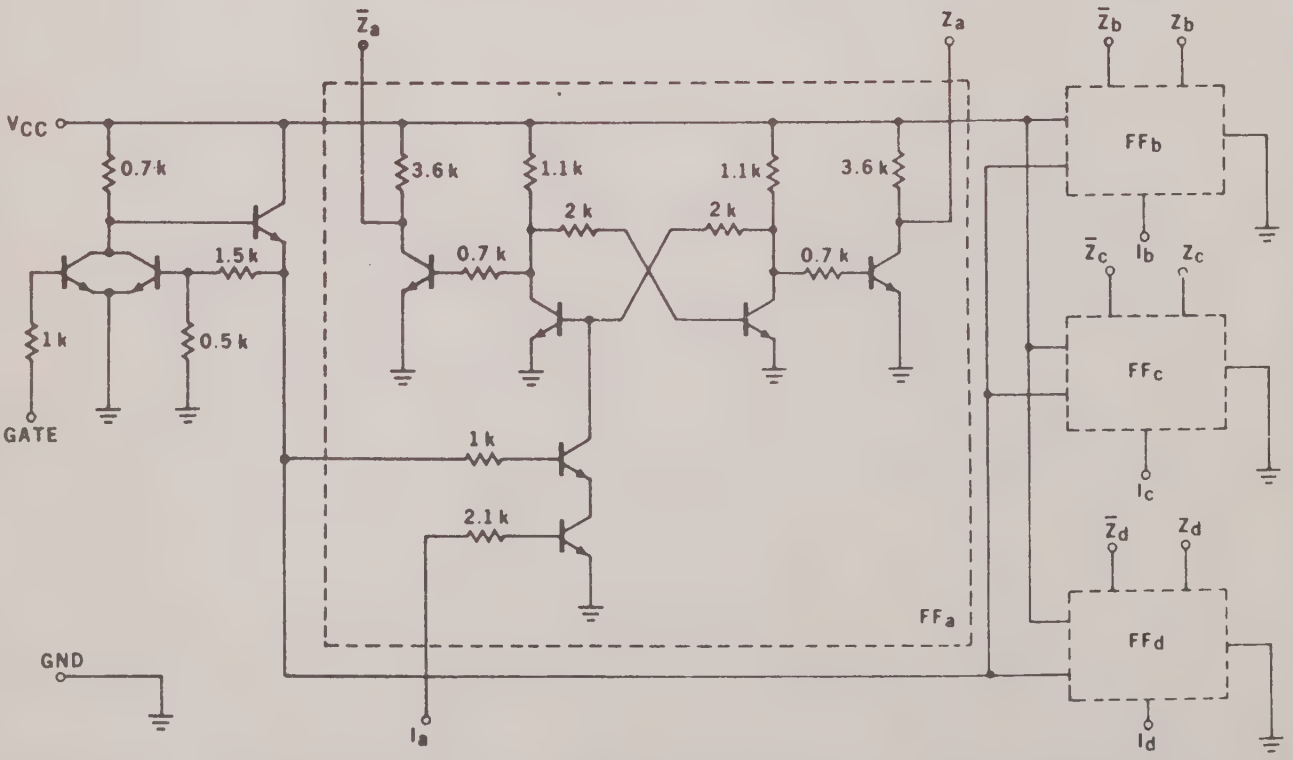


FIGURE 4-21

CμL 9959 EQUIVALENT

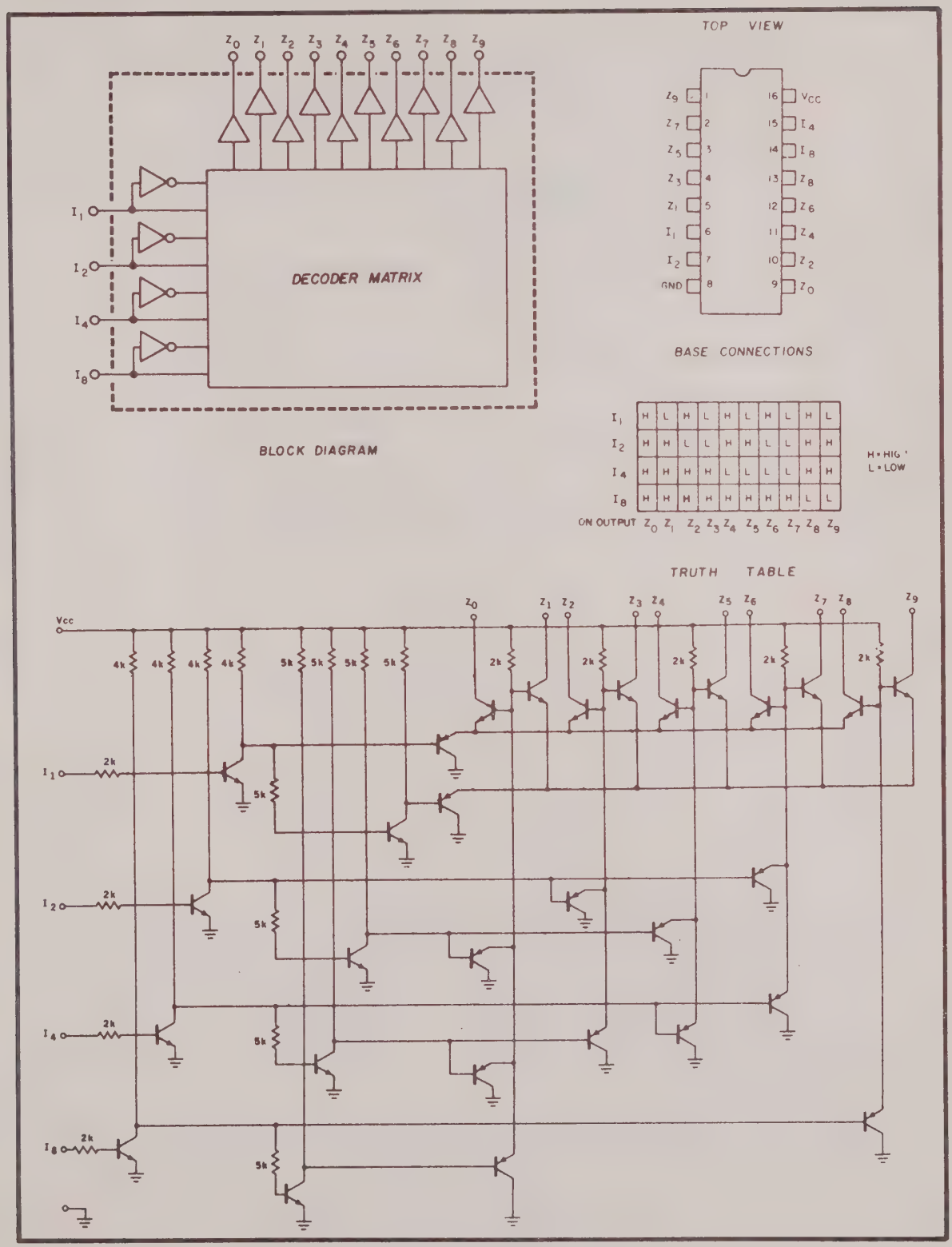
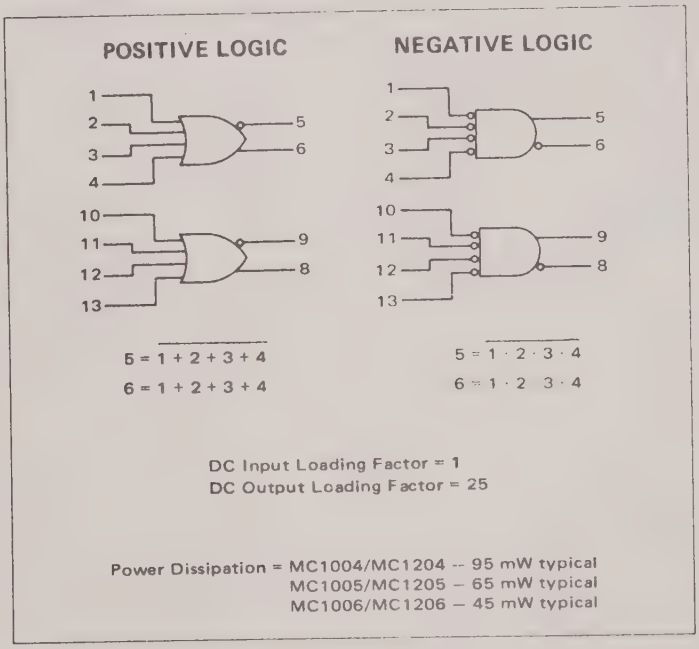


FIGURE 4-22

CμL 9960 EQUIVALENT

Provide simultaneous OR/NOR or AND/NAND output functions. These devices contain an internal bias reference insuring that the threshold point is always in the center of the transition region over the temperature range.

Emitter follower output configurations differ for these three circuits as shown in the circuit schematic.



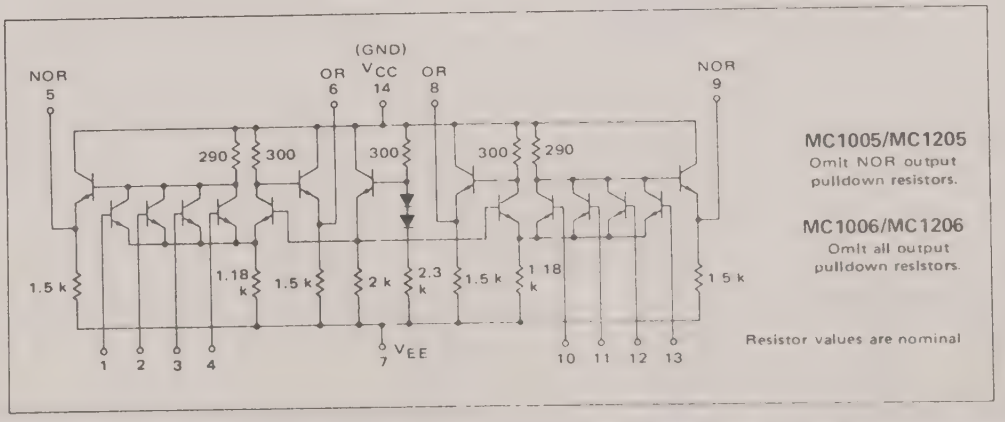
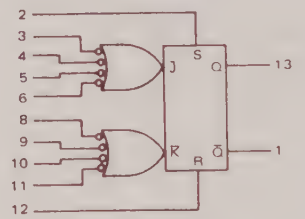


FIGURE 4-23

MC1004P(L) EQUIVALENT

Designed for use at clock frequencies to 70 MHz minimum (85 MHz typical). Logic performing inputs ($\bar{J}$ and $\bar{K}$) are available, as well as dc SET and RESET inputs.

POSITIVE LOGIC



DC Input Loading Factor = 1
DC Output Loading Factor = 25
Power Dissipation = 125 mW typical

* Any $\bar{J}$ or $\bar{K}$ input, not used for $\bar{C}_D$.
** $\bar{C}_D$ obtained by connecting one $\bar{J}$ and one $\bar{K}$ input together

The $\bar{J}$ and $\bar{K}$ inputs refer to logic levels while the $\bar{C}_D$ input refers to dynamic logic swings. The $\bar{J}$ and $\bar{K}$ inputs should be changed to a logical "1" only while the $\bar{C}_D$ input is in a logic "1" state. ($\bar{C}_D$ maximum "1" level = V_{CC} - 0.6 V). Clock $\bar{C}_D$ is obtained by tying one $\bar{J}$ and one $\bar{K}$ input together.

R S TRUTH TABLE

Pin No	R	S	Q^{n+1}
	12	2	13
	0	0	Q^n
	0	1	1
	1	0	0
	1	1	ND

All $\bar{J}$ $\bar{K}$ Inputs Are Static

$\bar{J}_D$ $\bar{K}_D$ TRUTH TABLE

Pin No	$\bar{J}_D$	$\bar{K}_D$	Q^{n+1}
	*	*	13
	1	0	Q^n
	0	1	0
	1	0	1
	1	1	$\bar{Q}^n$

All Other $\bar{J}$ $\bar{K}$ Inputs And The R S Inputs Are At a "0" Level

CLOCKED $\bar{J}$ $\bar{K}$ TRUTH TABLE

Pin No	$\bar{J}$	$\bar{K}$	$\bar{C}$	Q^{n+1}
	*	*	**	13
	Ø	Ø	0	Q^n
	0	0	1	$\bar{Q}^n$
	0	1	1	1
	1	0	1	0
	1	1	1	Q^n

All Other $\bar{J}$ $\bar{K}$ Inputs And The R S Inputs Are At a "0" Level

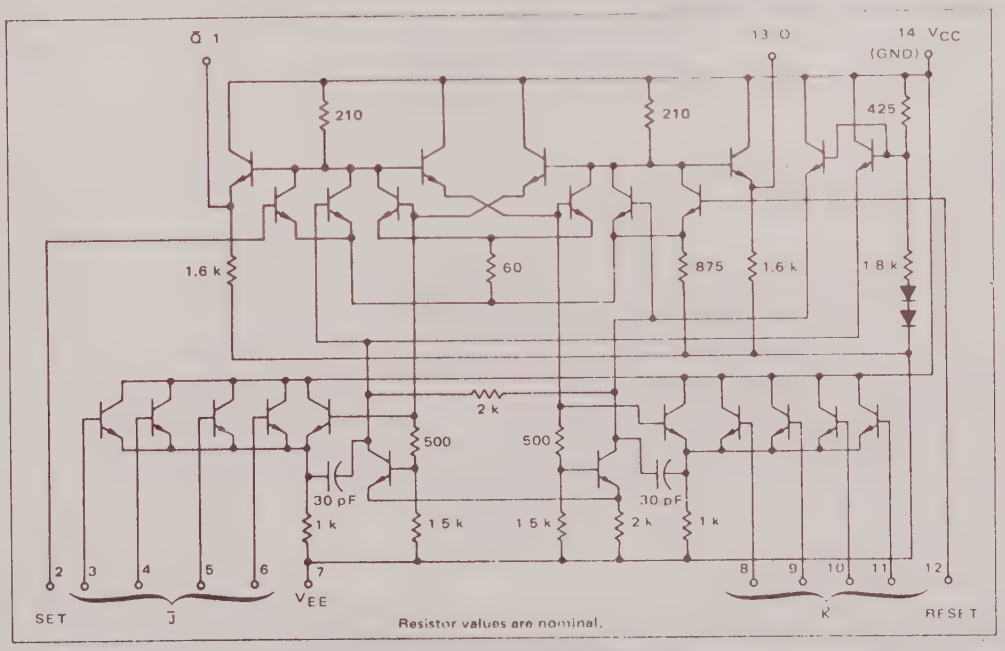
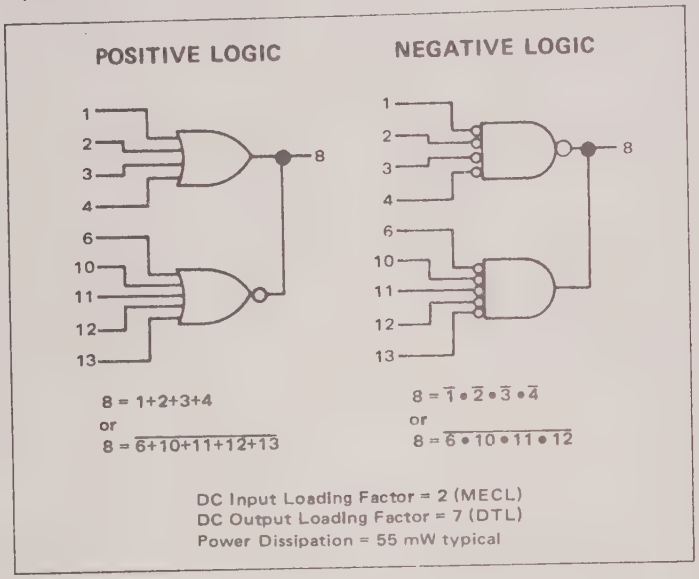


FIGURE 4-24

MC1013P(L) EQUIVALENT

Level translator intended for converting MECL signal levels to saturated logic levels. The translator will provide the positive logic OR or logic NOR function by connecting the internal bias driver output to the corresponding inputs of the differential amplifier. i.e., when pin 4 is connected to the reference bias, pin 5, pins 6, 10, 11 12, and 13 become the inputs of a 5-input NOR gate. When pin 6 is connected to the reference bias, pin 5, pins 1, 2, 3, and 4 become the inputs of a 4-input OR gate.



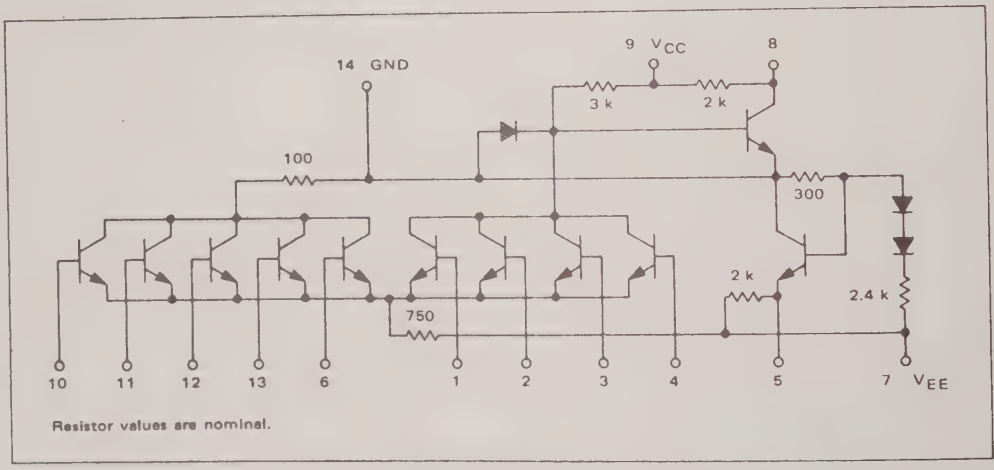
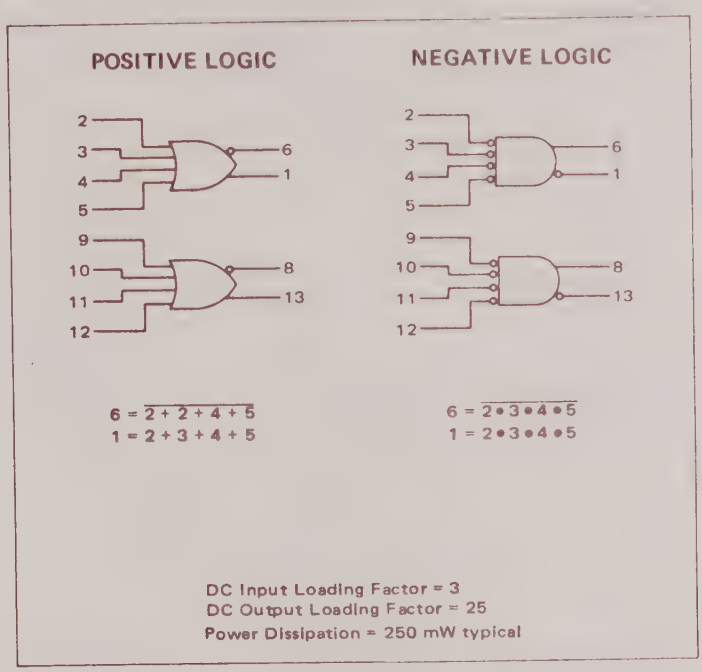


FIGURE 4-25

MC1018P(L) EQUIVALENT

Provides simultaneous OR/NOR or AND/NAND output functions. It contains an internal bias reference insuring that the threshold point is always in the center of the transition region over the temperature range.

This circuit is designed to operate in high-speed digital computer applications as a clock driver or as a high-speed gate.



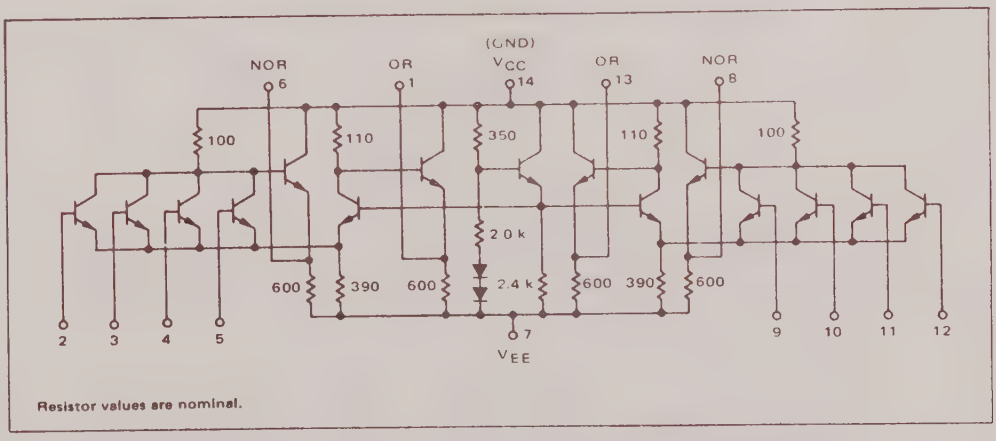
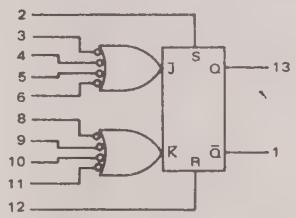


FIGURE 4-26

MC1023P(L) EQUIVALENT

Designed for use at clock frequencies to 100 MHz minimum (120 MHz typical). Logic performing inputs ($\overline{J}$ and $\overline{K}$) are available, as well as dc SET and RESET inputs.

POSITIVE LOGIC



DC Input Loading Factor = 2
DC Output Loading Factor = 25
Power Dissipation = 250 mW typical

R-S TRUTH TABLE

Pin No	R 12	S 2	Q^{n+1} 13
	0	0	Q^n
	0	1	1
	1	0	0
	1	1	N.D

All $\overline{J}$-$\overline{K}$ Inputs Are Static

$\overline{J}_D$-$\overline{K}_D$ TRUTH TABLE

Pin No.	$\overline{J}_D$ *	$\overline{K}_D$ *	Q^{n+1} 13
	0	0	Q^n
	0	1	0
	1	0	1
	1	1	$\overline{Q}^n$

All Other $\overline{J}$-$\overline{K}$ Inputs And The R-S Inputs Are At a "0" Level

CLOCKED $\overline{J}$ $\overline{K}$ TRUTH TABLE

Pin No.	$\overline{J}$ *	$\overline{K}$ *	$\overline{C}_D$ **	Q^n 13
	ϕ	ϕ	0	Q^n
	0	0	1	$\overline{Q}^n$
	0	1	1	1
	1	0	1	0
	1	1	1	Q^n

All Other $\overline{J}$-$\overline{K}$ Inputs And The R-S Inputs Are At a "0" Level

*Any $\overline{J}$ or $\overline{K}$ input, not used for $\overline{C}_D$.
**$\overline{C}_D$ obtained by connecting one $\overline{J}$ and one $\overline{K}$ input together.

The $\overline{J}$ and $\overline{K}$ inputs refer to logic levels while the $\overline{C}_D$ input refers to dynamic logic swings. The $\overline{J}$ and $\overline{K}$ inputs should be changed to a logical "1" only while the $\overline{C}_D$ input is in a logic "1" state. ($\overline{C}_D$ maximum "1" level = V_{CC} −0.6 V). Clock $\overline{C}_D$ is obtained by tying one $\overline{J}$ and one $\overline{K}$ input together.

CIRCUIT SCHEMATIC

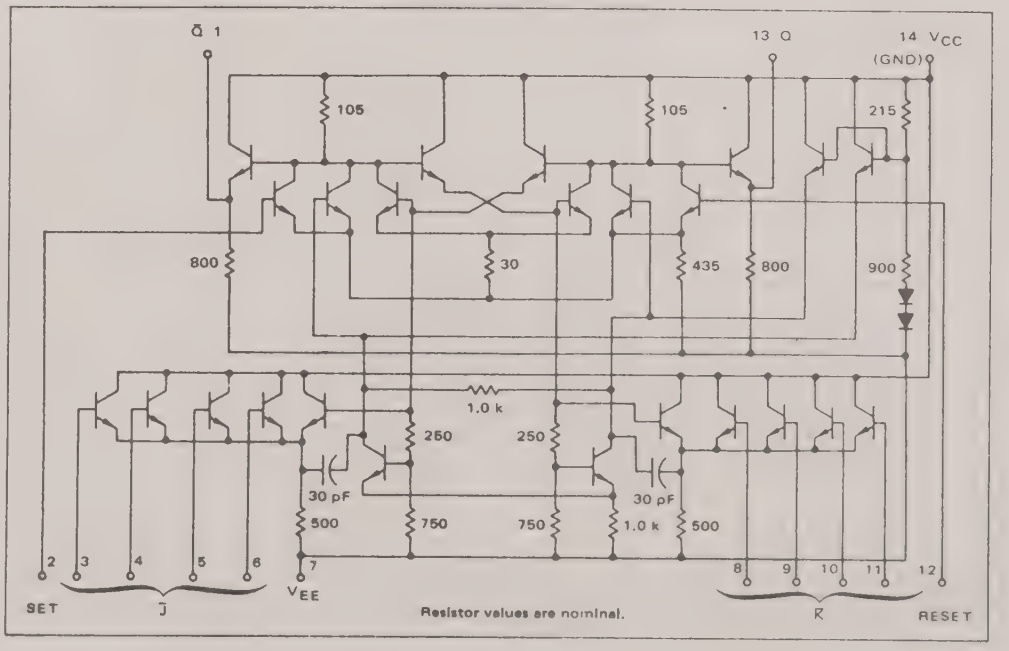


FIGURE 4-27

MC1027P(L) EQUIVALENT

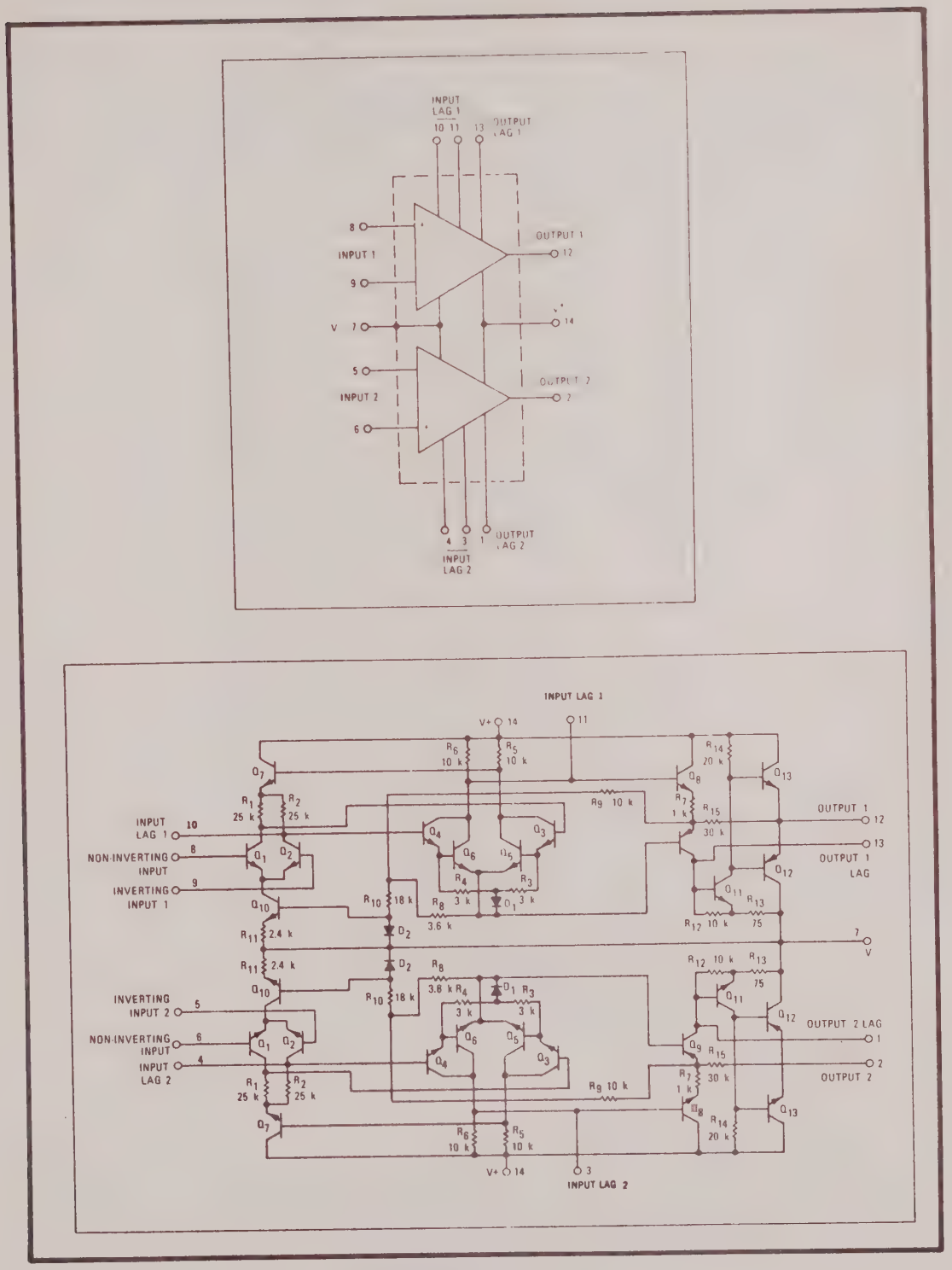


FIGURE 4-28

MC1437L EQUIVALENT

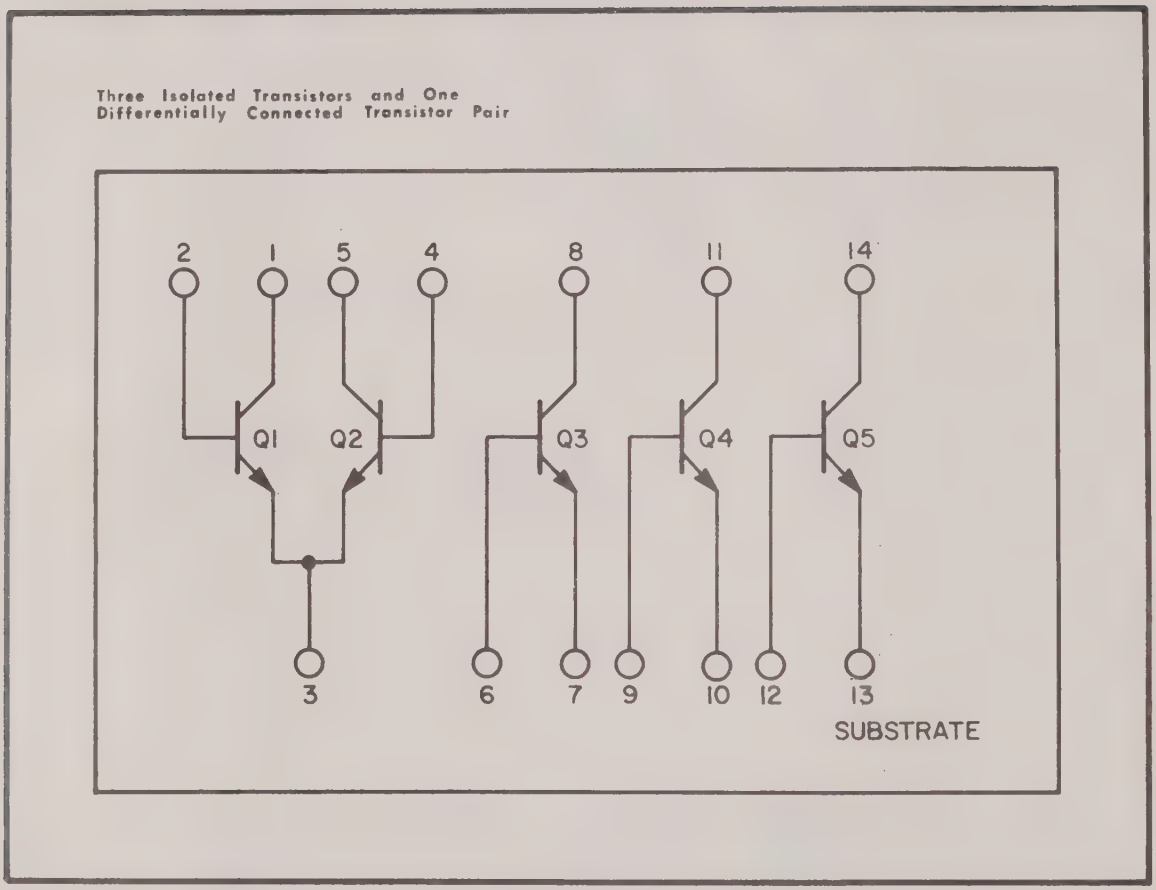


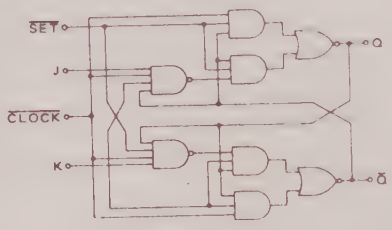
FIGURE 4-29

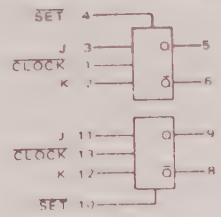
CA3046 EQUIVALENT

The MC3062 dual JK flip-flop triggers on the negative edge of the clock. Each flip flop is provided with a separate direct $\overline{SET}$ input. These direct inputs provide a means of presetting the flip-flop to initial conditions or other asynchronous operations.

Data may be applied to or changed at, the clocked inputs at any time during the clock cycle, except during the time interval between the Set up and Hold Times. The inputs are inhibited when the clock is low and enabled when the clock rises. The input steering network continuously responds to input information when the clock is high. The data state at the inputs throughout the interval between Set up and Hold time is stored in the flip flop when the clock falls. Each flip-flop may be set at anytime without regard to the clock state by applying a low level to the $\overline{SET}$ input.

LOGIC DIAGRAM
1/2 OF DEVICE SHOWN

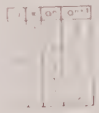




Input Loading Factors
$\overline{CLOCK}$, $\overline{SET}$ = 1.6
J, K, = 0.6

Output Loading Factor = 10

J-K TRUTH TABLE



Typical Characteristics
(V_{CC} = 5.0 V T_A = 25°C)

Total Power Dissipation = 100 mW/pkg
Toggle Frequency = 50 MHz
Logical "1" Setup Time = 8.0 ns
Logical "0" Setup Time = 8.0 ns
Logical "1" and "0" Hold Times = 0 ns
t_{pd} "1" = 12 ns
t_{pd} "0" = 12 ns

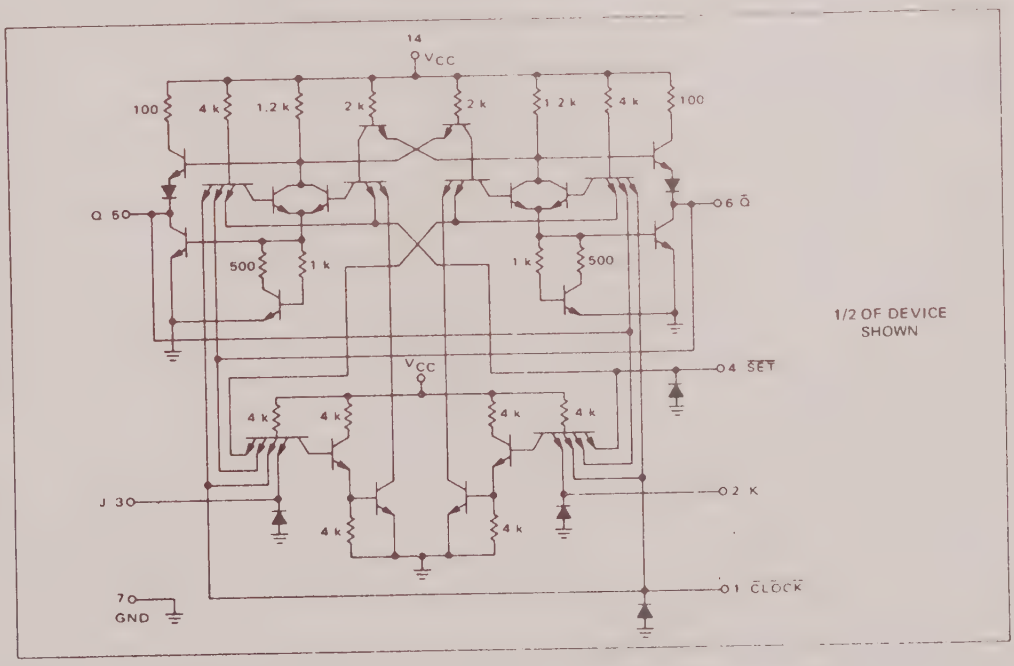


FIGURE 4-30

MC3062P(L) EQUIVALENT

SECTION 5

SCHEMATICS AND RELATED DRAWINGS

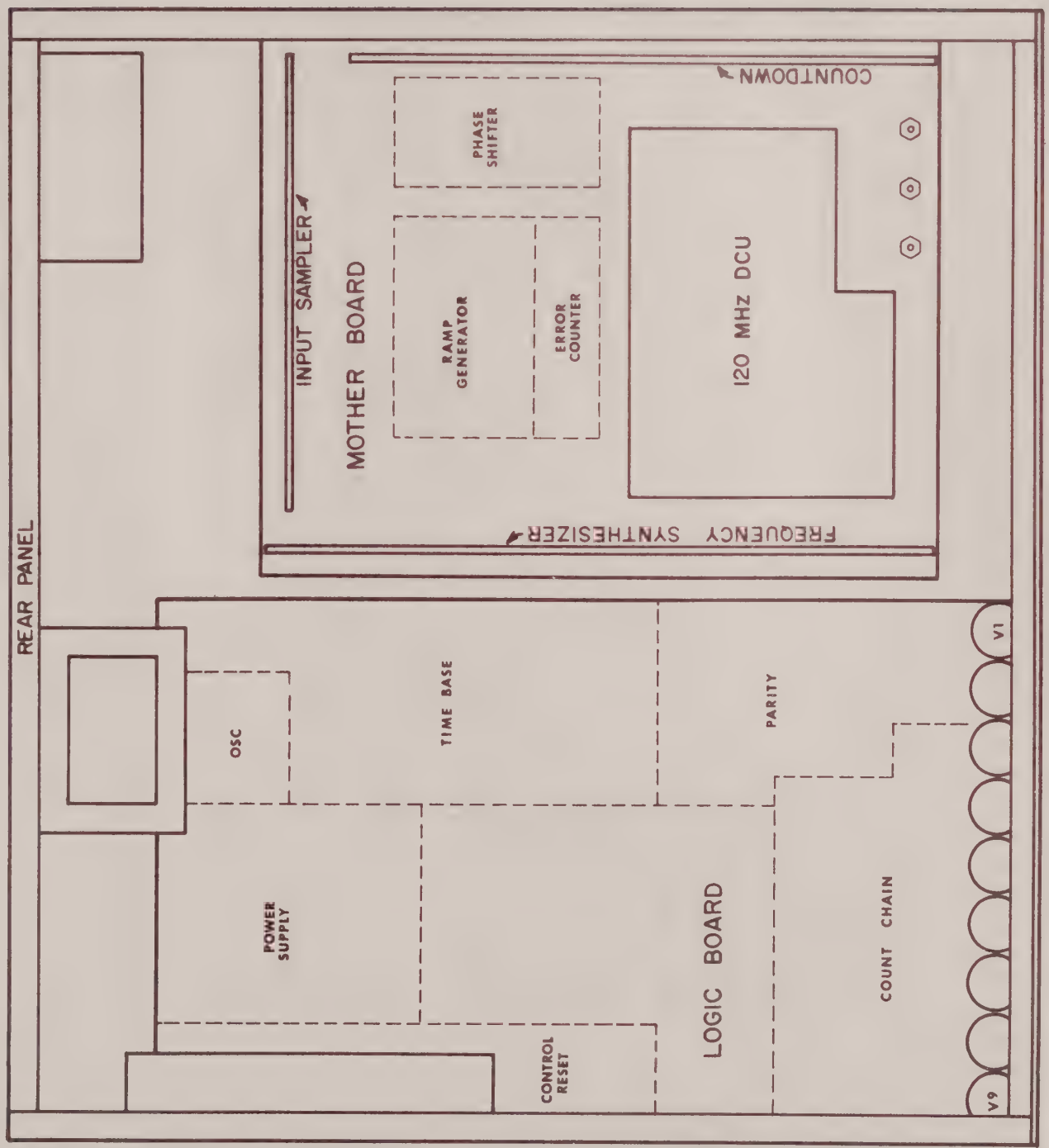


FIGURE 5-1

INTERNAL ORIENTATION

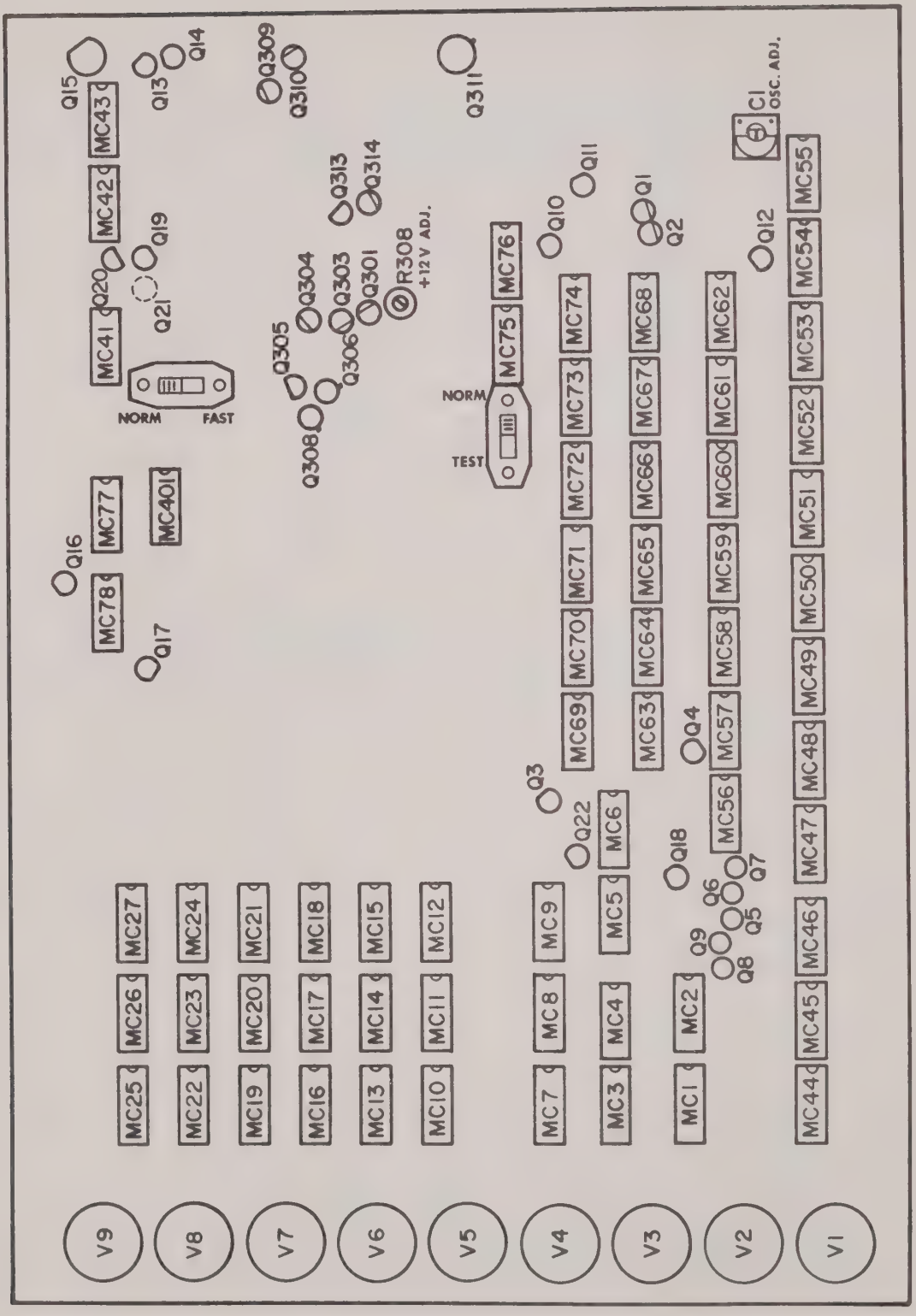


FIGURE 5-2

LOGIC BOARD COMPONENT LOCATION

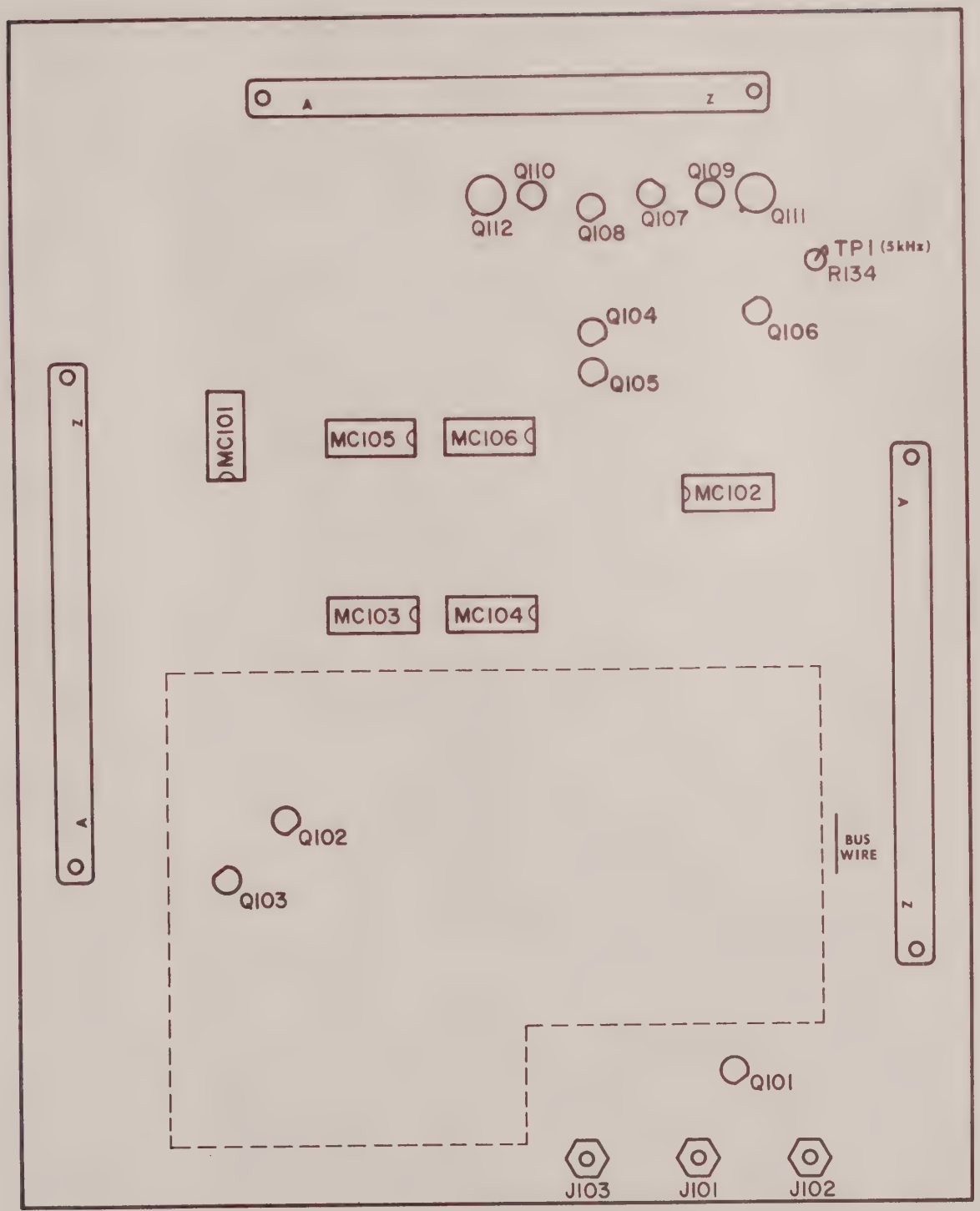


FIGURE 5-3

MOTHER BOARD COMPONENT LOCATION

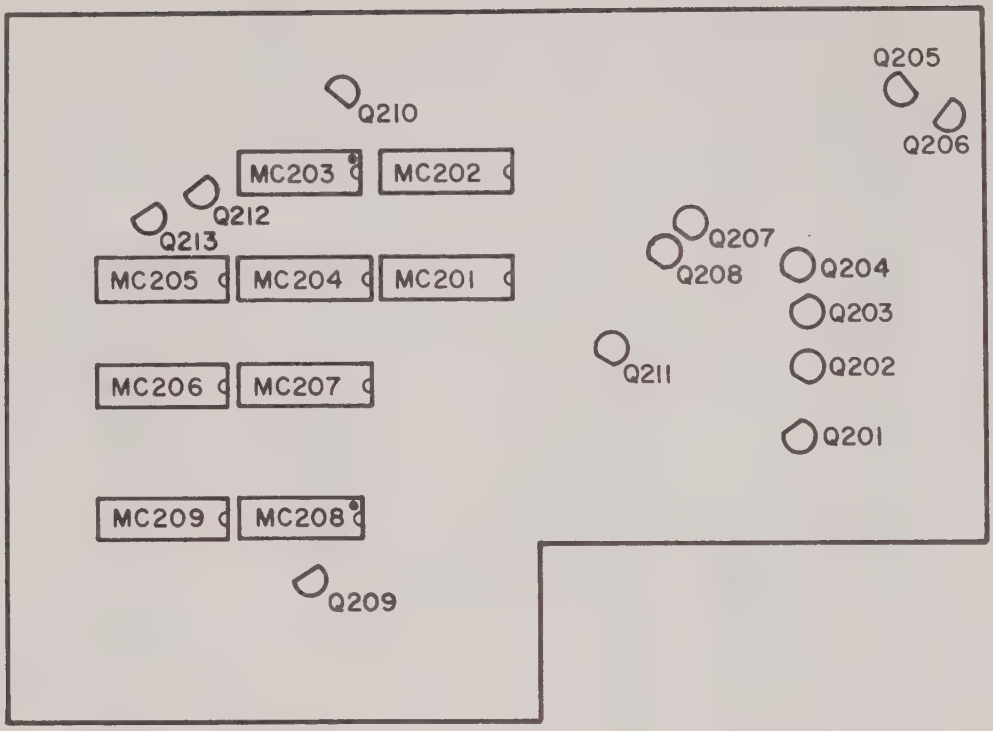


FIGURE 5-4

120 MHz DCU COMPONENT LOCATION

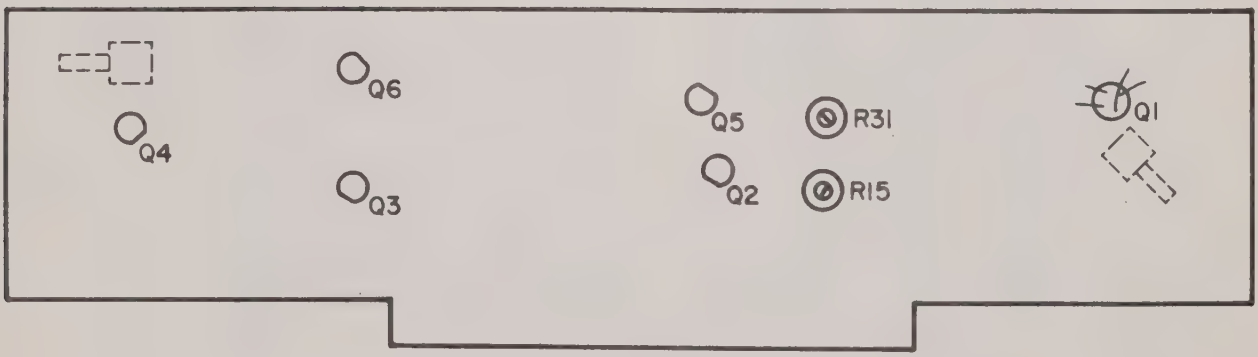


FIGURE 5-5

COUNTDOWN COMPONENT LOCATION

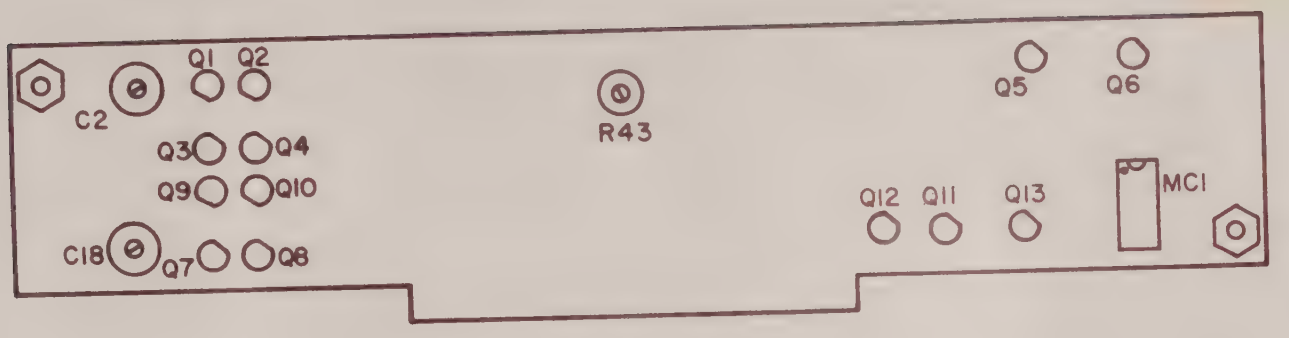


FIGURE 5-6

FREQUENCY SYNTHESIZER COMPONENT LOCATION

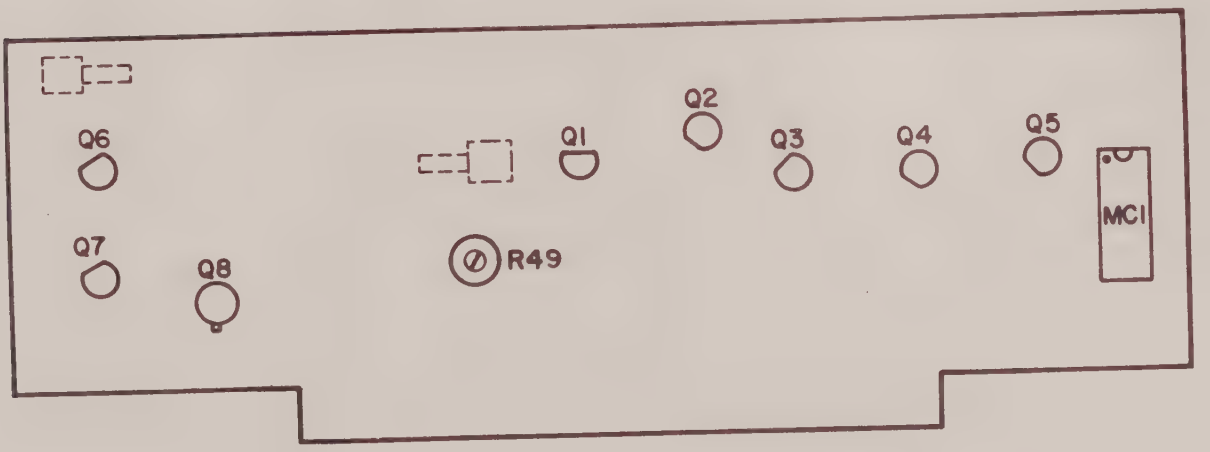


FIGURE 5-7

INPUT SAMPLER COMPONENT LOCATION

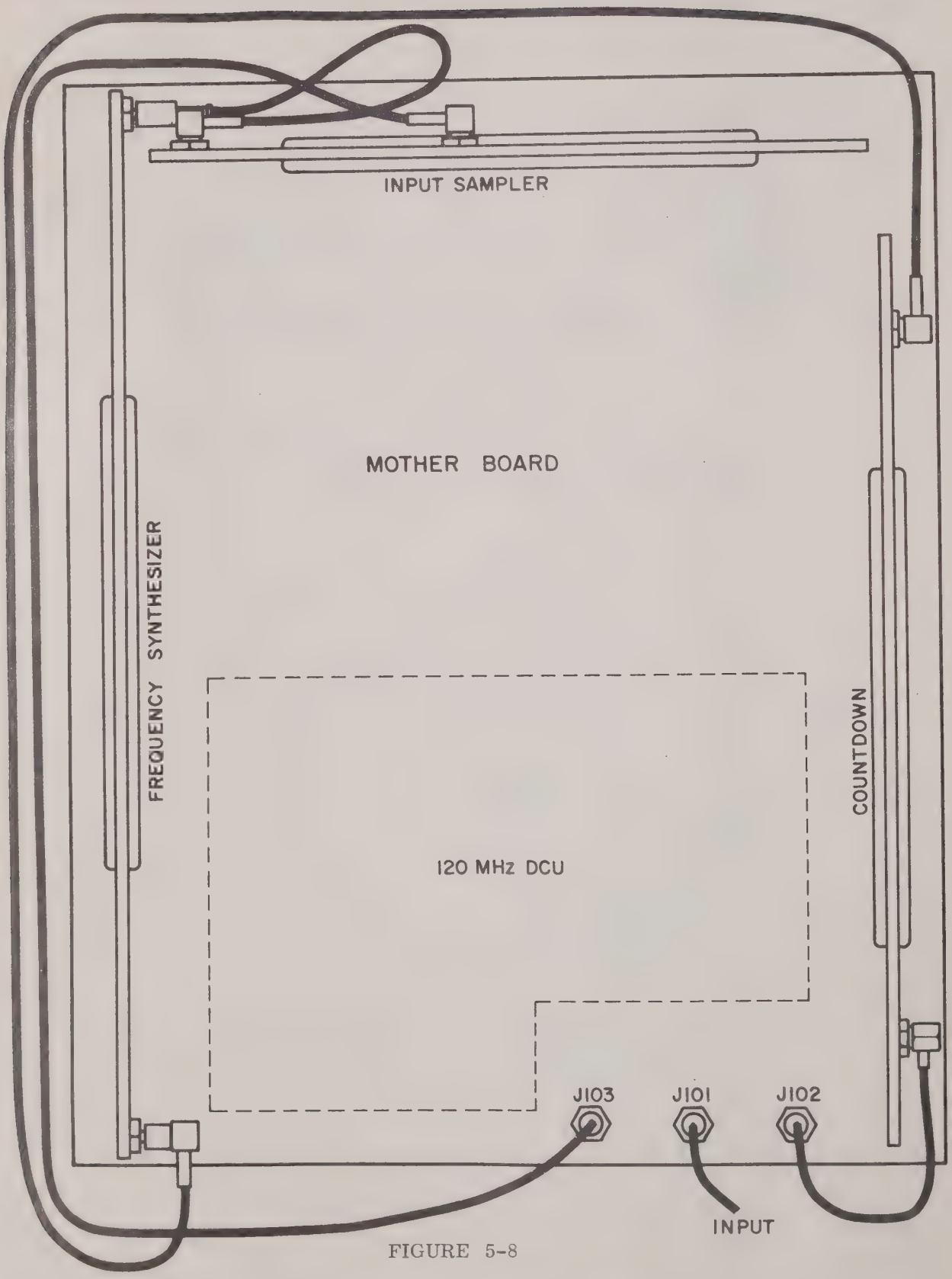


FIGURE 5-8

COAXIAL CABLE TERMINATIONS

REV	DESCRIPTION	ECO	BY	DATE	CHKD

+12 V
R169 4.7Ω
R170 4.7Ω
R171 1K
Q109 2N3640
Q111 2N4890
M̄
R172 1K
-12 V
+4.5V
R174 1K
Q107 2N3646
R173 106Ω
H
M
L
Q110 2N3640
R179 1K
R180 4.7Ω
R181 4.7Ω
Q112 2N4890
H̄
R182 1K
-12 V
Q108 2N3646
MC101A MC724P
TEST
OVERIDE
+4.5V
+4.5V
R163 47Ω
+4.5V
CR101 IN3605
+3.8V
MC101B MC724P
MC101C MC724P
L+T
PC3 CH4 GND-CC
RTL RESET
R111 470Ω
Q103 2N3646
R110 4.7K
+4.5V
C104
R109 5.6Ω
Q102 2N3640
R108 1K
-5.2V
R107 27Ω
MECH RESET
J102 TO CD
R101A 100Ω
R101B 100Ω
J101 INPUT
R103 220Ω
R104 100Ω
Q101 2N4275
R105 10Ω
+12V
C103 .1μf
C101 2.5pf
R102A 100Ω
R102B 100Ω
TC DIRECT BAND
R106 2.7K
J103 TO IS
-12 V

ITEM	DESCRIPTION	PART NO OR MAT'L	REV	MFG OR FINISH	ENG	QUAN	QUAN REQD	MFG
WORK ORDER	QUAN START	FCR	DATE	ECR	DATE	ECR	DATE	

ELDORADO ELECTRONICS
CONCORD CALIFORNIA

TOLERANCES UNLESS NOTED
ELECTRICAL
ALL RESISTORS ¼ WATT 5% ALL TRANSISTORS ALL CAPACITORS ALL DIODES
MECHANICAL
.XX = ± .005 .XXX = ± .005 DIMENSIONS ARE IN INCHES
HOLE DIA ± .005 ANGLES ±1°
BREAK SHARP EDGES, BURRS AND TOOL MARKS

SCALE NONE
DO NOT SCALE THIS DRAWING

DRW BY
CK BY
APP BY
APP BY

DATE 7-9-67
DATE 8-1-67
DATE
DATE

TITLE INPUT AMP POWER DIVIDER AND MISC. CONTROL CIR.
MODEL 970
DWG NO C-11-06052

NEXT ASSEMBLY | MODEL

REV.	DESCRIPTION				

R8 1.8K

C5 .001μf

CR2 IN3605

L2 .82 μh

R12 10Ω

R13 120

R15 200

CR3 IR754A

R18 100Ω 1/2W

C15 0.1

+12V

R17

C16 .1 μf

C -

R24 2.2K

C17

INPUT FROM POWER DIVIDER

C 15μf

R1 10K 1/8W

R3 27Ω 1/8 W

R23 1.8K

CR6 IN3605

C22

L12 33μh

+12V

0.1μf

33μh

-12V

0.1μf

L7

2N3640

IN3605

R32, 47Ω 1/2W

R33

0.2JL

100JL

IN 754A

0.1μf

EN2894A

-12V

ITEM	DESCRIPTION	PART NO OR MATL	QTY	INFO ON FINISH	CHG	CHAR	DRAW REVS	SIZE

WORK ORDER	DRAWN / START	ECR	DATE	ECR	DATE	ECR	DATE

ELDORADO ELECTRONICS
CONCORD CALIFORNIA

TOLERANCES UNLESS NOTED
ELECTRICAL
ALL RESISTORS ¼ WATT 5% ALL TRANSISTORS
ALL CAPACITORS ALL DIODES
MECHANICAL
.00 = ± .01 HOLE DIA ± .005
.000 = ± .005 ANGLES ±1°
DIMENSIONS ARE IN INCHES
KEEP FREE FROM SCRATCHES BURRS AND TOOL MARKS

SCALE

DO NOT SCALE THIS DRAWING

DRW BY
CK BY
APP BY
APP BY

DATE 7-9-
DATE 8-5-
DATE 2-17-
DATE 1-16-

TITLE SCHEMATIC, 5 WATT AMP

MODEL 970

SIZE A DWG NO C-11 06A717

REV A

NEXT ASSEMBLY | MODEL

REV.	DESCRIPTION	ECO	BY	DATE	CHKD

L8 100μh +12V C35 .1μf C36 10μf

L9 100μh -12V C37 .1μf C38 10μf

M

R44 820Ω

R3 3.9K

R4 56Ω

C3 10pf

T1 3T 6T

C1 150pf

C3 7-25

R1 330Ω 3T

R2 330Ω

C.W. INPUT FROM COUNTDOWN

+12V

M

R12 1K

CR1 CR2

L1 2.2μh

MC1B 3062

+12V

R14 820Ω

CR11 1N4152

R29 1K

R30 2.2K

L5 0.82μh

L6 1.2μh

L7 0.82μh

C39 .005μf

C38 40μf 15V

R21 3.9K

R24 56Ω

Q7 2N3640

Q8 2N3640

T5 3T GT

C17 22pf

C18 3-15 pf

R19 390Ω 3T

R20 180Ω

H

C19 .01μf

R22 3.9K

R26 360Ω

R27 68Ω

C21 .005μf

Q9 2N3640

Q10 2N3640

T6 3T

CR7

C22 .005μf

T7 3T

R32 27Ω

C41 .01μf

R39 3.3K

R42 470Ω

C43 82pf

Q11 2N3640

Q12 2N3640

Q13 2N3646

R33 22Ω

R34 1K

C31 .005μf

ITEM	DESCRIPTION	PART NO OR MAT'L	REV	MFG OR FINISH	CHG	QUAN	QUAN REQD	LES

WORK ORDER QUAN START ECR DATE ECR DATE ECR DATE

ELDORADO ELECTRONICS CONCORD, CALIFORNIA

TOLERANCES UNLESS NOTED: ELECTRICAL ALL RESISTORS ½ WATT OR ALL TRANSISTORS ALL CAPACITORS ALL DIODES MECHANICAL .00 = ± .010 .000 = ± .005 ANGLES ± 1° BREAK SHARP EDGES AND REMOVE BURRS KEEP FREE FROM SCRATCHES DURRS AND TOOL MARKS

SCALE NONE DO NOT SCALE THIS DRAWING

DRN BY LRS DATE 4-6-67

CK BY DATE 8/69

APP BY DATE

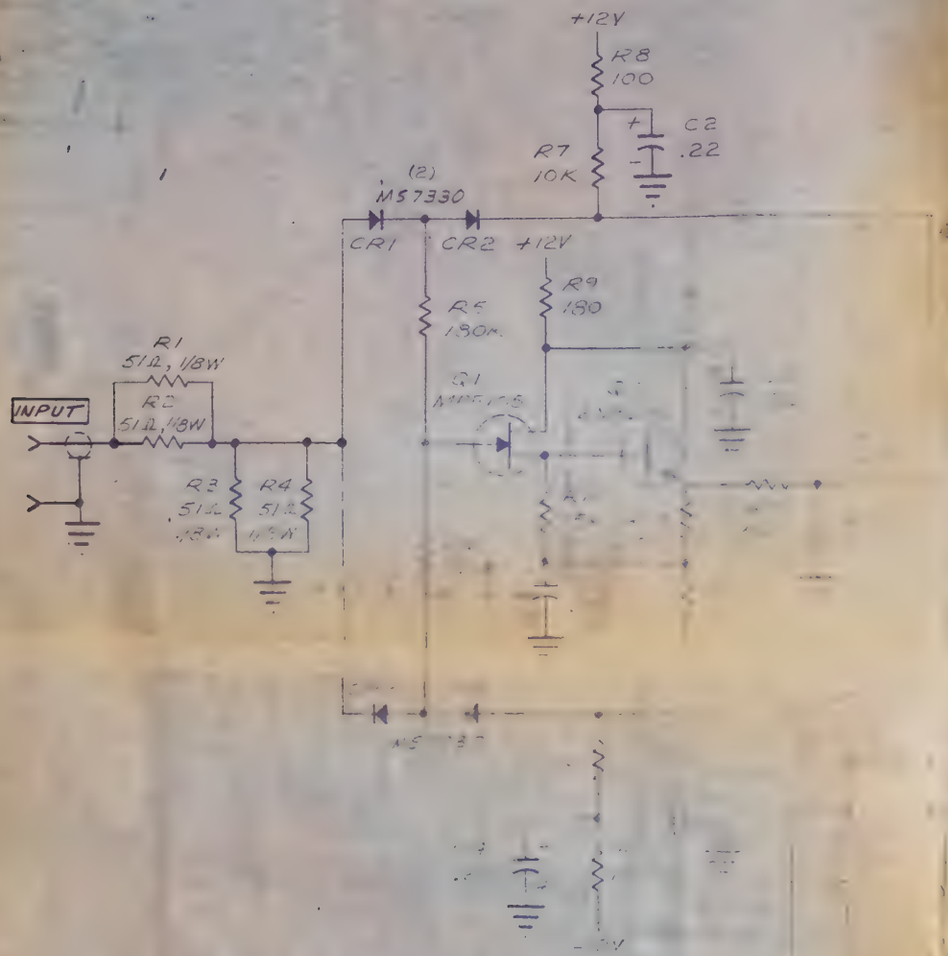
APP BY DATE

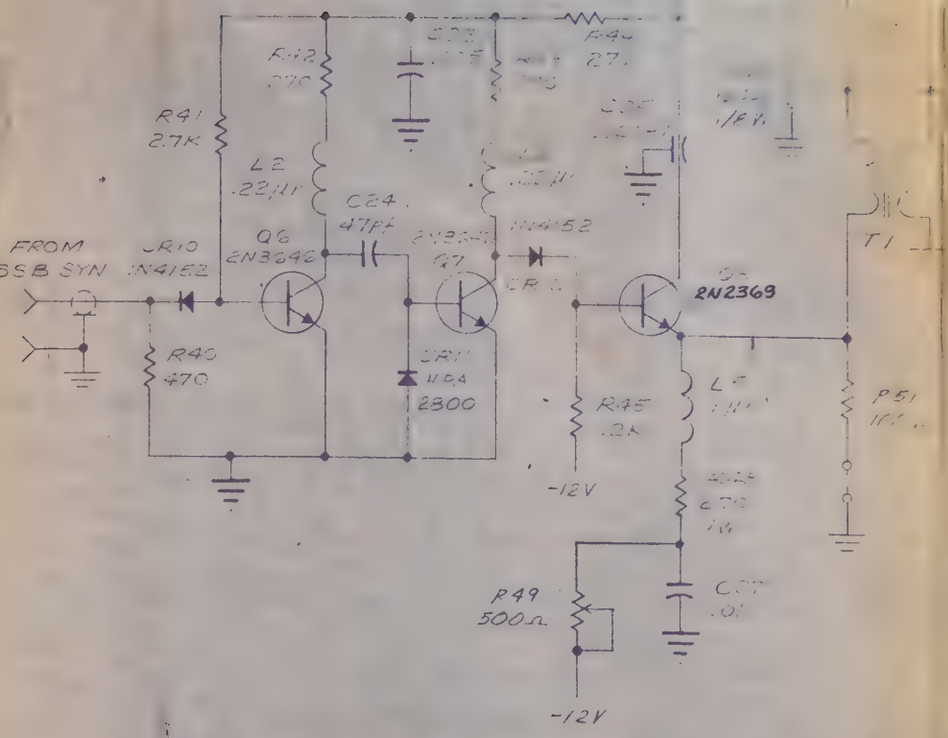
TITLE SCHEMATIC, FREQUENCY SYNTHESIZER

MODEL 970 DWG NO C 11-0701 A

NEXT ASSEMBLY MODEL

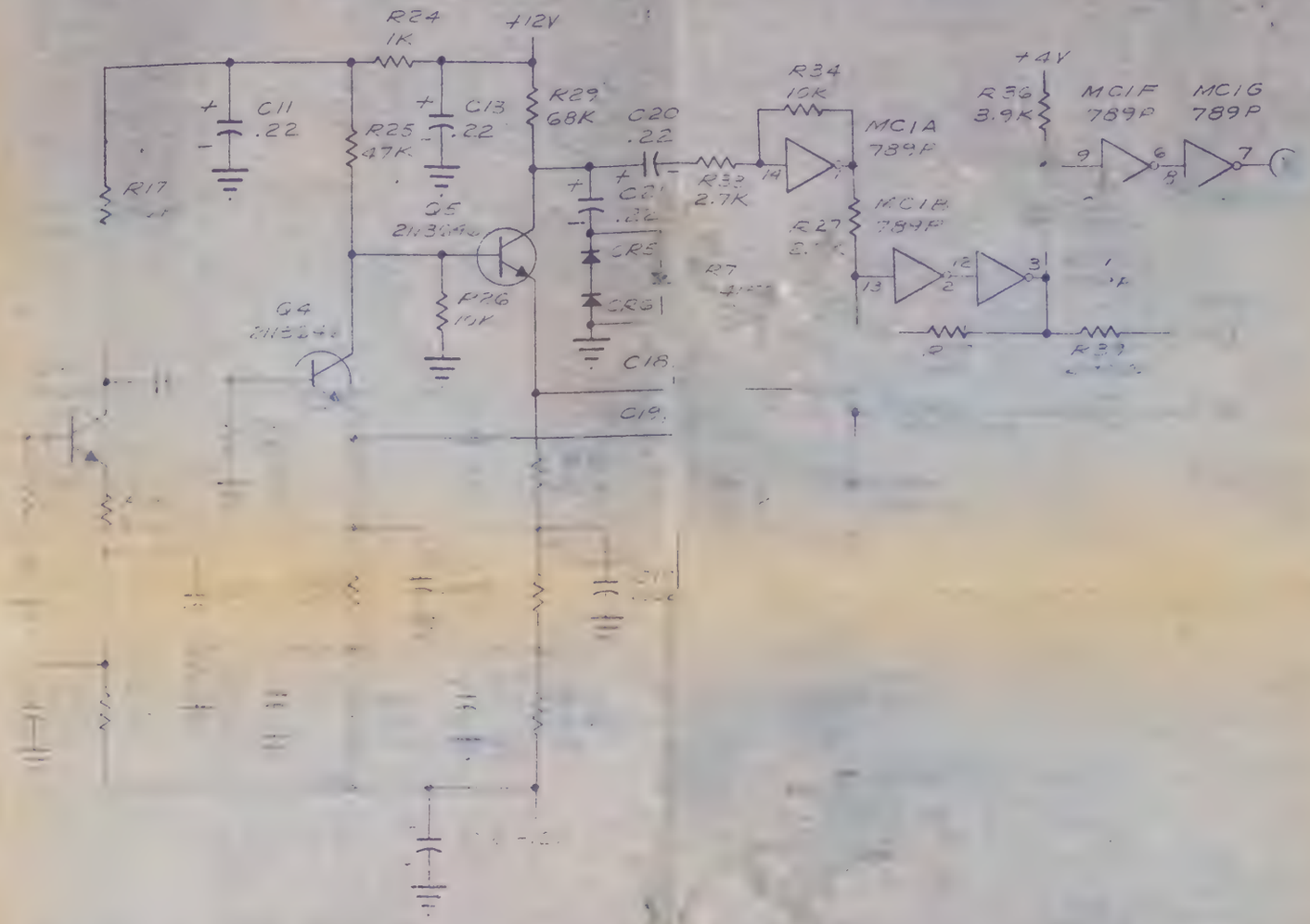
REV	DESCRIPTION	ECO	BY	DATE

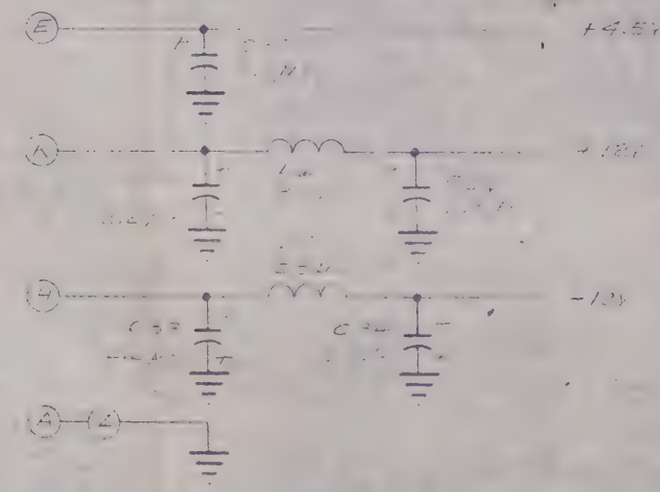




NOTES:

1. SPECIAL INDUCTORS, SEE INSTRUCTION MANUAL.





ITEM	DESCRIPTION	PART NO OR MAT'L	REV	INFO OR FINISH	CHG	QUAN	QUAN REQ	SEE
WORK ORDER	ISSUE / START	ECR	DATE	ECR	DATE	ECR	DATE	

ELDORADO ELECTRONICS
CONCORD CALIFORNIA

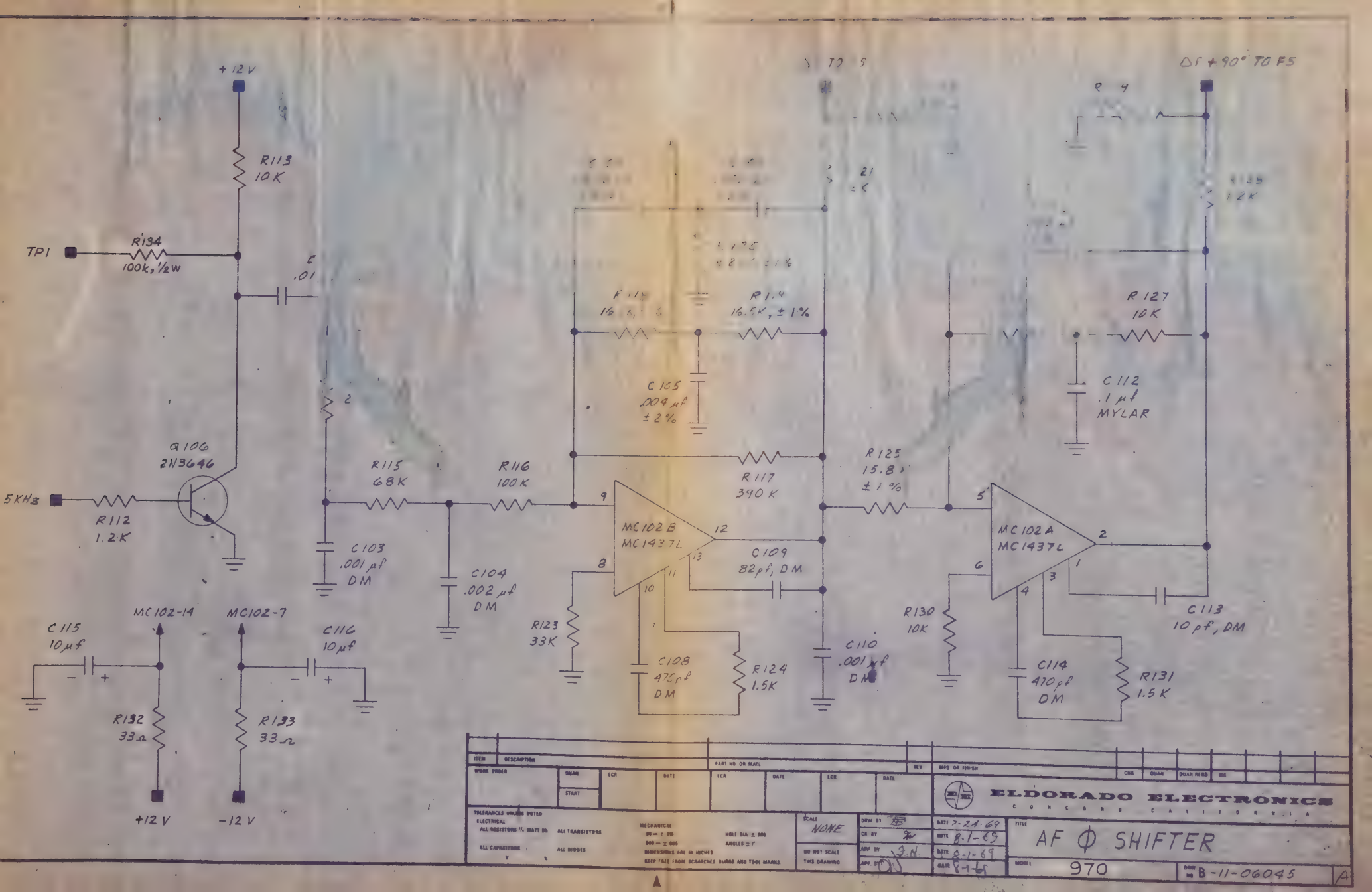
TOLERANCES UNLESS NOTED
ELECTRICAL
ALL RESISTORS ½ WATT 5% ALL TRANSISTORS
ALL CAPACITORS ALL DIODES
MECHANICAL
.00 = ± .005
.000 = ± .005
HOLE DIA ± .004
ANGLES ± 1°
DIMENSIONS ARE IN INCHES
KEEP FREE FROM SCRATCHES BURRS AND TOOL MARKS

SCALE NONE
DO NOT SCALE THIS DRAWING

DRN BY LRG DATE 4-7-69
CK BY DATE 6-1-69
APP BY DATE
APP BY DATE 9-1-69

TITLE SCHEMATIC, SAMPLER
MODEL 970
C 11-05823 A

NEXT ASSEMBLY | MODEL


+12 V
R113
10K
TP1
R134
100k, ½w
C
.01
Q106
2N3646
5KHz
R112
1.2K
R115
68K
R116
100K
C103
.001 µf
DM
C104
.002 µf
DM
MC102-14
MC102-7
C115
10µf
C116
10µf
R132
33Ω
R133
33Ω
+12 V
-12 V
C105
.004 µf
±2%
R117
390 K
MC102B
MC1437L
C109
82pf, DM
R123
33K
C108
470pf
DM
R124
1.5K
C110
.001 µf
DM
R125
15.8K
±1%
MC102A
MC1437L
R130
10K
C114
470pf
DM
R131
1.5K
C113
10 pf, DM
R127
10K
C112
.1 µf
MYLAR
ELDORADO ELECTRONICS
CONCORD CALIFORNIA
AF Φ SHIFTER
970
B-11-06045
A

REV	DESCRIPTION	ECO	BY	DATE	CHKD

+12V

L102
1 mh

C118
50 µf
15 V

R135
3.75K
±1%

R136
3.75K, ±1%

R137
7.5K
±1%

R139
7.5K
±1%

R140
3.75K, ±1%

MC105
CA3046

R141
7.5K
±%

R142
3.75K, ±1%

R143
7.5K
±1%

R144
3.75K, ±½%

R145
7.5K
±½%

R158
470Ω

R166
220Ω

MC106
30Ω

Q103
2N3906

R146
10K
±%

-12V

L101
1 mh

C117
50 µf
15 V

CR104
IN4152

RAMP
(TO ROUTING BOARD)

R164
1.8K

ERROR
RESET
(SEARCH SIGNAL)

MC103A
MC791P

MC103B
MC791P

MC104
MC839P

+4.5 V

R165
10Ω

ITEM	DESCRIPTION	PART NO OR SHEET	REV	MFG OR FINISH	CWG	DOAR	QUAN REQD	RQ

WORK ORDER	DWAR	ECR	DATE	ECR	DATE	ECR	DATE
	START						

ELDORADO ELECTRONICS
CONCORD CALIFORNIA

TOLERANCES UNLESS NOTED
ELECTRICAL
ALL RESISTORS ½ WATT 5% ALL TRANSISTORS
ALL CAPACITORS ALL DIODES
V %
MECHANICAL
.00 = ± .015 HOLE DIA ± .005
.000 = ± .005 ANGLES ± 1°
DIMENSIONS ARE IN INCHES
KEEP FREE FROM SCRATCHES, BURRS AND TOOL MARKS

SCALE NONE
DO NOT SCALE THIS DRAWING

DRW BY
CA BY
APP BY
APP BY

DATE 7-25-69
DATE 8-1-69
DATE 8-1-69
DATE 8-1-69

TITLE ERROR COUNTER AND RAMP GENERATOR

MODEL 970

DRW NO C-11-C6046 A

NEXT ASSEMBLY | MODEL

REV	DESCRIPTION	ECO	BY	DATE	CHKD

PAR 1 PAR 2 PAR 4 PAR 8

R39 560Ω R40 560Ω R41 560Ω

MC 52 P

MC51A MC725P

MC50C MC724P

TB BAND ERROR

+3.6V

R46 2.7K

C16 .002μf

800 μS

MC51B MC725P

MC50D MC724P

MC

MC 72

C18 .1μf

+3.6V

R36 2.7K

MC55A MC790P

MC62D MC789P

200μS

MC 72 P

RESET

C17 .002μf

MC55B MC790P

MC INPUT

MC49D MC724P

+3.6V

R51 2.2K

C20 .01μf

MC44A MC717P

TB HO

MC48B MC790P

FPEP 1

RESET

+3.6V

R34 10K R35 820Ω

MC47D MC717P

MC62F MC789P

MC47B MC717P

R54 680Ω

DISPLAY

R55 1K C14 .01μf

Q12 2N3646

800mS

C15 470pf

MC54B MC717P

MC44D MC717P

MC44C MC717P

MC47A MC717P

R47 680Ω

.01μf

MC54C MC717P

R37 4.7K

MC44A MC717P

R48 3.9K

CR3 IN695 CR4 IN695 CR5 IN695

R53 4.7K

+3.6V

1mS

"N"

MC54A MC717P

RESET

8mS

MC45C MC717P

MC45D MC717C

MC 46 CμL953

R38 390Ω

MC44B MC724P

NOTES:

1. DESIGNATIONS
   - ▲ TO LOG'S BOARD - TIME BASE
   - ● TO CONTROL, RESET
   - ■ TO POWER SUPPLY & OFF BOARD

ITEM	DESCRIPTION	PART NO OR MATL	REV	MFG OR FINISH	CDG	GUARD	GUARD RECD	VEE
WORK ORDER	GUARD START	ECR DATE	ECR DATE	ECR DATE				

TOLERANCES UNLESS NOTED
ELECTRICAL
ALL RESISTORS ¼ WATT 5% ALL TRANSISTORS
ALL CAPACITORS ALL DIODES
MECHANICAL
.00 = ± .015 HOLE DIA ± .005
.000 = ± .005 ANGLES ± 1°
DIMENSIONS ARE IN INCHES
KEEP FREE FROM SCRATCHES, BURRS AND TOOL MARKS

SCALE NONE
DO NOT SCALE THIS DRAWING

DRWN BY
CK BY
APP BY
APP BY

DATE 7-17-69
DATE 8-1-69
DATE 8-1-69
DATE 7-17-69

ELDORADO ELECTRONICS
CONCORD CALIFORNIA

TITLE FINE AND COARSE PARITY

MODEL 970

DRW NO C-11-C6049 A

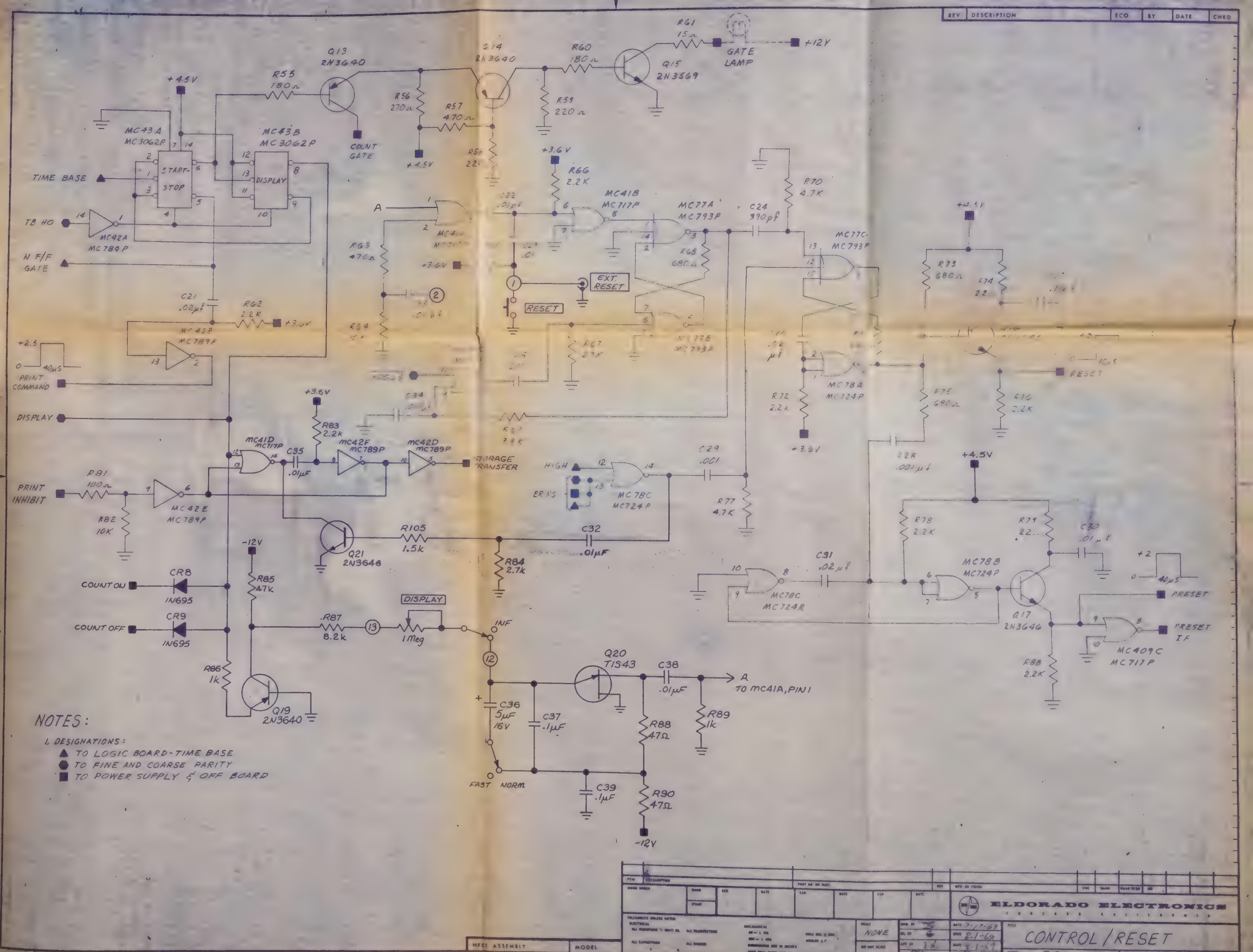
NEXT ASSEMBLY

RESOLUTION
1MS
10MS
100MS
1S
10S
+3.6V
R16 1.5K
DEC.1
Q5 4-1007
R17 1.5K
DEC.2
Q6 4-1007
R18 1.5K
DEC.3
Q7 4-1007
R19 1.5K
DEC.4
Q8 4-1007
R20 1.5K
DEC.5
Q9 4-1007
R15 1.K
MC71B MC717P
MC66D MC717P
MC66B MC786
LOW BAND ENABLE (MODE/RANGE SWITCH)
MC72A MC717P
MC72C MC717P
MC71C MC724
MC66B MC717P
MC56A MC717P
MC56C MC717P
MC66B MC786
MC71D MC724
MC71A MC724
C8 470pf
TB OUTPUT F/F MC70A MC724
R22 470Ω
R23 470Ω
+3.6V
MC67 CμL125
MC68 CμL958
RESET
MC59A MC717
5KHz TO AF ϕ
8mS
MC58 CμL958
MC57 CμL958
RESET
MC56B MC717P
MC69 CμL958
RESET
MC63 CμL958
RESET
R21 820Ω
+3.6V
MC61 CμL958
MC60 CμL958
MC62A MC724
MC62B MC724
MC59D MC717
500 KHz
MC56D MC717
MC56B MC717
MC56C MC717
R10 220Ω
MC45B MC717
1mS
R12 1K
MC64 MC9721P
MC73 MC9721P
PRESET
MC59C MC717P
800μS
Q4 2N3646
R13 1.K
C12 390
R91 2.7K
CR1 IN270
D42 2.2V
+3.6V
CR2 IN270
MC72B MC724
TB BAND ERROR
+3.6V
C9 270
MC74B MC717
R26 4.7K
MC74C MC717
R27 4.7K
C10 270
MC43A PIN 5 (N F/F GATE)
+3.6V
R25 6.8K
MC74A MC717
T
N
TEST-NORMAL
ER RS
MC70C MC724
MC74D MC717
"N"
R29 1.5K
Q10 2N3646
+3.6V
R30 3.3K
PAR 1
PAR 2
PAR 4
MC76 CμL958
RESET
PAR 8
MC75 CμL958
RESET
R31 930Ω
R32 1.5K
+3.6V
R33 3.3K
Q11 2N3646
N > 8
C5 470pf
R1 47K
C3 .1
C4 .01
R4 3.3K
R3 2.7K
R2 100Ω
C6 .02μ
Q2 2N2926
Q1 2N2926
C40 .01
1 MHz
C2 22pf N750
C1 1-12pf
R7 5.6K
R8 1.K
R9 2.2K
+3.6V
R14 2.2K
+3.6V
R24 3.3K
MC43B MC717
MC74A MC717

NOTES:
1. DESIGNATIONS:
- TO FINE AND COARSE PARITY
- TO CONTROL/RESET
- OFF BOARD

ELDORADO ELECTRONICS
CERRITOS CALIFORNIA
DRAWN BY 7-19-67
CHK BY 8-1-67
APP BY 8-1-67
DATE 8-1-67
NONE
LOGIC BOARD-TIME BASE
970
D-11-06044

REV	DESCRIPTION	ECO	BY	DATE	CHKD



NOTES:

1. DESIGNATIONS:
   - ▲ TO LOGIC BOARD - TIME BASE
   - ⬢ TO FINE AND COARSE PARITY
   - ■ TO POWER SUPPLY & OFF BOARD

NEXT ASSEMBLY	MODEL

ELDORADO ELECTRONICS
CONCORD CALIFORNIA

SCALE: NONE
DRWN BY: [illegible] 7-7-69
CHK BY: [illegible] 8-1-69
APP BY: T.H. 8-1-69
DATE: [illegible]

TITLE: CONTROL / RESET
MODEL: 970
DWG NO: C-11-00048
REV: A

REV	DESCRIPTION	ECO	BY	DATE	CHKD

DIRECT INPUT
C201 .01μ
R203 180Ω
R204 91Ω
R207 330Ω
R208 200Ω
C218 50μf 12V
Q201 2N3563
Q202 2N3640
C203 22pf
Q204 2N3640
Q203 2N3563
R201 430Ω
R255 68Ω
C202 22pf
R205 220Ω
R206 130Ω
C204 22pf
CR201 IN3605
CR202 IN3605
R202 2.7K
Q206 2N[illegible]2
R212 820Ω
C206 2500μf
C207 .1μf
C208 330pf
C212 .1μf
R211 910Ω
C209 .01μf
+12V
-5.2V
-12V
L202 1μh
L203 1μh
C216 5μf, 15V
C217 5μf 15V
+3.6V
1 MHz TEST SIG.
MC203B MC724P
MC203D MC724P
MC203C MC724P
MC203A MC724P
CH. A ENABLE
TEST OVERIDE
R240 820Ω
R234 1K
R235 10K
R232 1.5K
R233 10K
R227 2.2K
R226 1K
CR210 IN3605
R225 5.1K
R228 22K
R229 22K
Q212 2N3702
Q213 2N3702
MC202A MC1004P
MC202B MC1004P
MC202C MC1004P
MC202D MC1004P
MC202E MC1023P
MC202F MC1023P
CR211 IN3605
R222 22K
R223 1.5K
R224 10K
R230 270Ω
R231 68Ω
Q210 2N3702
C210 GATE
L201 1μh
C211 .1μf
R214 1000Ω
C205 22pf
R217 68Ω
Q207 EN2894A
Q208 EN2894A
CR207 IN3605
R213 33Ω
R215 510Ω
R216 330Ω
R218 196Ω
R210 [illegible]
CR203 IN3605
CR204 IN3605
CR205 IN3605
CR206 IN3605
C213 .01μf
R236 1K
Q211 2N3640
R237 2K
R238 390Ω
R239 100Ω
C214 100pf
C215 .015μf
FROM COUNTDOWN
P256 330Ω
P257 150Ω
R247 4.7K
MC204 MC1013P
MC205 MC1013P
MC206 MC1013P
MC207 MC1013P
R241 4.7K
R242 4.7K
R243 4.7K
R244 4.7K
R245 10K
RESET
MC208B MC717P
MC208A MC717P
MC209 MC1018P
12 MHz INPUT
TO CUSTOMER (COUNT CHAIN)
CR208 IN3605
R220 220Ω
R246 510Ω
R221 180Ω
CR209 IN3605
Q209 2N3702
C[illegible] .01μf

NEXT ASSEMBLY | MODEL

ELDORADO ELECTRONICS
CONCORD CALIFORNIA

SCALE NONE
DRWN BY
CK BY
APP BY
APP BY
DATE 7-29-69
DATE 8-1-69
DATE 8-1-69

TITLE 120 MHz DCU
MODEL 970
DWG NO C-11-06051 A

V1 NL848 — R93 47k 1/2W — DEC. 1
V2 NL848 — R94 47k 1/2W — DEC. 2
V3 NL848 — R95 47k 1/2W — DEC. 3
V4 NL848 — R96 47k 1/2W — DEC. 4
V5 NL848 — R97 47k 1/2W — DEC. 5
V6 NL848 — R98 47k 1/2W
V7 NL840 — R99 47k 1/2W
V8 NL840 — R100 47k 1/2W
V9 NL840 — R101 47k 1/2W

MC1 CμL9960 — MC2 CμL9959 — MC3 CμL9960 — MC4 CμL9959 — MC7 CμL9960 — MC8 CμL9959 — MC9 CμL9958 — MC10 CμL9960 — MC11 CμL9959 — MC12 CμL9958 — MC13 CμL9960 — MC14 CμL9959 — MC15 CμL9958 — MC16 CμL9960 — MC17 CμL9959 — MC18 CμL9958 — MC19 CμL9960 — MC20 CμL9959 — MC21 CμL9958 — MC22 CμL9960 — MC23 CμL9959 — MC24 CμL9958 — MC25 CμL9960 — MC26 CμL9959 — MC27 CμL9958

RTL RESET

MC5A — MC5B

+4.5V

R102 2.2K — R103 2.2K — R104 680Ω

CR6 IN3605 — CR7 IN3605

C41 .1μF

Q18 2N3646

Q22 2N3646 — R106 820Ω — +4.5V — R105 2.2K

RTL RESET

ELDORADO ELECTRONICS

DRAWN GARY — DATE 10/14/70

SCHEMATIC, COUNT CHAIN

970

REV.	DESCRIPTION	ECO	BY	DATE	CHKD

CR301 IN2071
R301 120Ω
230V
C301 8μf, 350V
R302 220K, ½W
C306 .01μf
MDA 920A-2
CR303 CR304 CR302 CR305
28.5 VRMS C.T.
C311 1000μf 25V
C302 1,000μf 25V
C303 1,000μf 25V
S301 POWER
F301 1A SB
S302 115/230V
B301
FL 301
J301
Q301 2N2924
Q302 MJE 520
R303 220Ω
R304 220Ω
Q303 2N2924
Q304 2N2924
R306 .68Ω, 1W
R305 820Ω
R307 199Ω ±1%
R308 100Ω CERMET BOURN
R309 274Ω ±1%
CW
CR310 IN754A 6.8V
8.3V
CR307 IN1612
CR308 IN1612
CR306 CR309
MDA940A-2
C304 8,000μf 12V
14.5 VRMS C.T.
C308 1,000μf 25V
8.3V
T301
12V
R318 390Ω
R317 1K
12V, @ 400ma
C307 500μf, 15V
R310 1K
CR311 IN3605
CR312 IN3605
R311 1K, ±1%
C308 500μf 15V
12V
Q305 2N3702
Q306 2N706
R312 220Ω
Q307 MJE520
Q308 2N706
R315 220Ω
R313 10K
R314 220Ω
R316 1.5Ω ½W
8.3V
Q311 2N3053
Q312 40251
R320 220Ω
R321 220Ω
R322 .18Ω 2W
Q309 2N2924
R319 150Ω
Q310 2N2924
CR313 IN748A, 3.9V
CR315 IN4001
3.6V
4.4V, ±5% @ 1.8A
C309 500μf 15V
C310 500μf 15V
5.2V
R325 220Ω
CR314 IN695
Q316 MJE 520
Q313 2N3702
R323 221Ω, ±1%
R327 220Ω
R328 1.2Ω ½W
R324 274Ω ±1%
R326 1K
Q314 2N2924
12V
8.3V

ITEM	DESCRIPTION	PART NO. OR SHEET	REV.	MFG. OR VENDOR	CHG	QUAN	QUAN NEED	USE
WORK ORDER	QUAN START	ECR	DATE	ECR	DATE	ECR	DATE	

TOLERANCES UNLESS NOTED: ELECTRICAL — ALL RESISTORS ¼ WATT 5% ALL TRANSISTORS; ALL CAPACITORS V S ALL DIODES; MECHANICAL .XX ± .01 .XXX ± .005 MILS DIA ± .005 ANGLES ±1°; DIMENSIONS ARE IN INCHES; KEEP FREE FROM SCRATCHES, BURRS AND TOOL MARKS

SCALE NONE — DO NOT SCALE THIS DRAWING

DWN BY — DATE 7-17-69
CK. BY — DATE 8-1-69
APP. BY J.H. — DATE 8-1-69
APP. BY — DATE 8-1-69

ELDORADO ELECTRONICS
CONCORD, CALIFORNIA

TITLE: LOGIC BOARD, POWER SUPPLY
MODEL 970
DWG. NO. C-11-06047 A

NEXT ASSEMBLY | MODEL

www.manualsplus.com
1012402